



# DLPC900 Digital Controller for Advanced Light Control

## 1 Features

- One scalable controller supports both DLP6500 and DLP9000 DMDs for high resolution industrial and display applications
- Supports 1080p and WQXGA capabilities of DLP6500 and DLP9500, respectively
- Supports multiple high-speed pattern rates
  - 1-Bit Binary Patterns Rates up to 9500 Hz
  - 8-Bit Gray Patterns Rates up to 250 Hz
  - 1-to-1 Input Mapping to Micromirrors
  - Multiple Bit Depth and LEDs in Pattern Modes
  - 128 MB Internal DRAM Stores up to 400 1-Bit Binary Patterns
  - 48 MB External Flash Stores up to 250 1-Bit Binary or 30 8-Bit Gray Patterns
- Easy Synchronization With Cameras and Sensors
  - Two Configurable Input Triggers
  - Two Configurable Output Triggers
- Fully Programmable GPIO and PWM Signals
- Multiple Control Interfaces
  - One USB 1.1 Slave Port and three I<sup>2</sup>C Ports
  - LED Enable and PWM Generators
- Video Projection Mode
  - 24-Bit RGB Rates up to 120 Hz
  - YUV, YCrCb, or RGB Data Format
  - Two 30-Bit Input Pixel Ports
  - Standard Video from SVGA to 1080p
  - WQXGA up to 120Hz with DLP9000 (requires 2x DLPC900)
- Integrated Clock and Micromirror Drivers

## 2 Applications

- Industrial
  - 3D Machine Vision and Quality Control
  - 3D Printing
  - Direct Imaging Lithography
  - Laser Marking and repair
- Medical
  - Ophthalmology
  - 3D Scanners for Limb and Skin Measurement
  - Hyper-spectral Scanning
- Displays
  - Intelligent and Adaptive Lighting
  - 3D Imaging Microscopes

## 3 Description

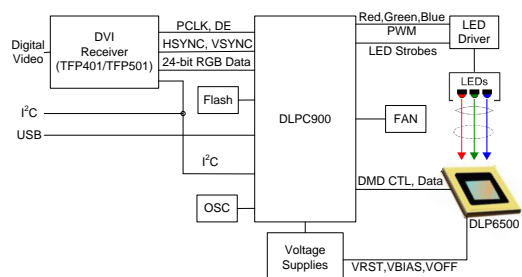
The DLPC900 is a single scalable DMD (digital micromirror device) controller that supports reliable operation of three high resolution DMD chips: DLP6500FLQ, DLP6500FYE, and DLP9000FLS. This high performance DMD controller enables programmable, high speed pattern rates for advanced light control especially in industrial, medical and scientific applications. DLPC900 pattern rates enable fast and accurate 3D scanning and 3D printing, as well as support high resolution and intelligent imaging applications. DLPC900 offers 128MB of embedded DRAM for convenient storage of up to 400 1-bit patterns. Input and output triggers are offer easy connection and synchronization with a variety of cameras, sensors or other peripherals. Numerous ports and connectivity options offer system flexibility and simplify chip integration into a variety of end equipment.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC900ZPC	BGA (516)	27.00 x 27.00 mm

(1) For all available packages, refer to the orderable addendum at the end of the data sheet.

### Simplified Diagram



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## 4 Revision History

DATE	REVISION	NOTES
October 2014	*	Draft release.

## 5 Pin Configuration and Functions

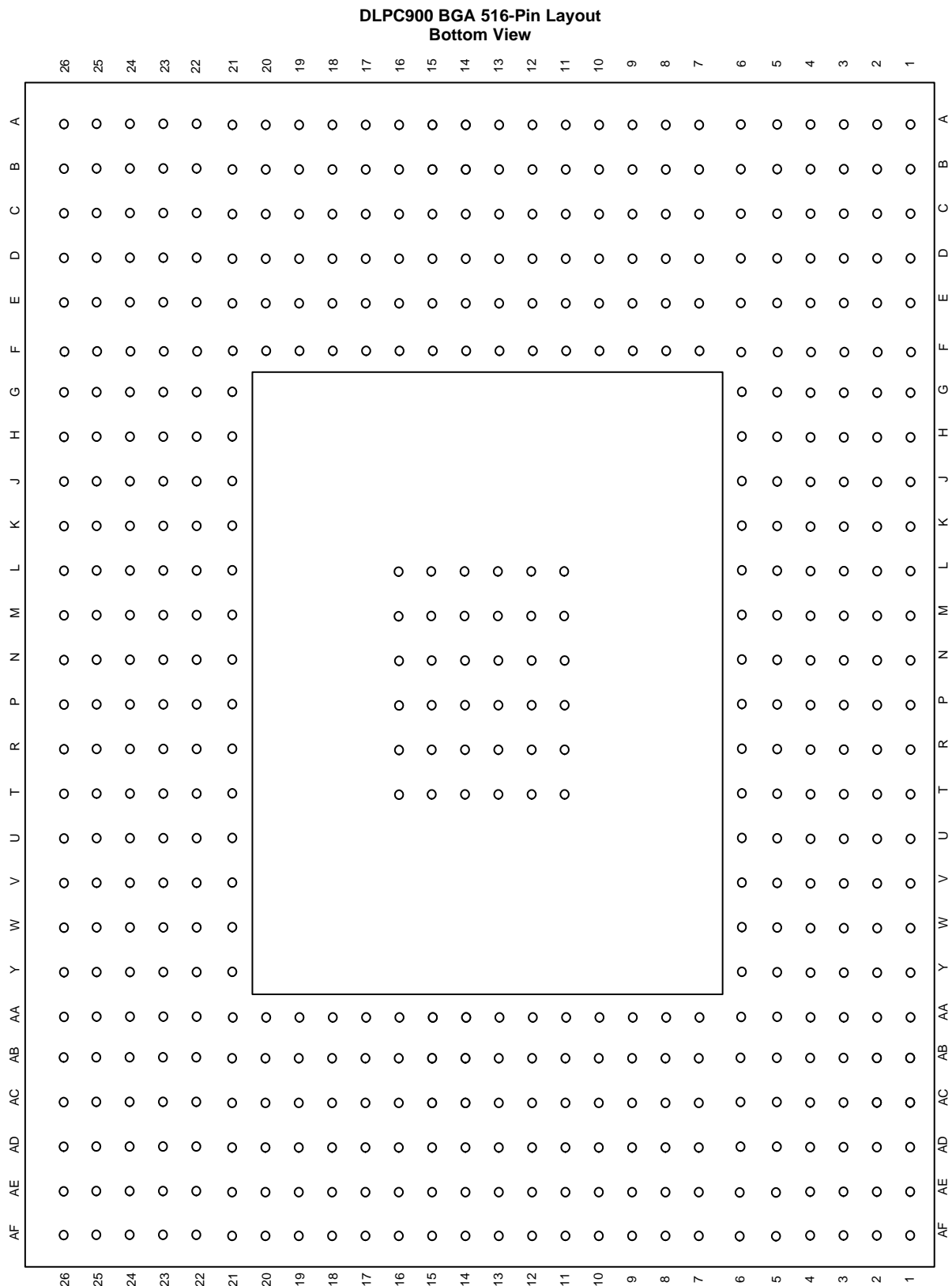


Table 1 contains the I/O Type and Subscript definitions found in the Pin Function tables.

Refer to the [General Handling Guidelines for Unused CMOS-type Pins](#) for instructions on handling unused pins

**Table 1. I/O Type and Subscript Definition**

I/O		ESD STRUCTURE
(SUBSCRIPT)	DESCRIPTION	
1	N/A	N/A
2	3.3 LVTTTL I/O buffer, with 8-mA drive	ESD diode to V <sub>DD33</sub> and GND
3	3.3 LVTTTL I/O buffer, with 12-mA drive	
4	3.3 LVTTTL receiver	
5	3.3 LVTTTL I/O buffer, with 8-mA drive, with slew rate control	
6	3.3 LVTTTL I/O buffer, with programmable 4-, 8-, or 12-mA drive	
7	1.8-V LVDS (DMD interface)	
8	3.3-V I <sup>2</sup> C with 3-mA sink	
9	USB-compatible (3.3 V)	
10	OSC 3.3-V I/O compatible LVTTTL	
(TYPE)		N/A
I	Input	
O	Output	
B	Bidirectional	
H	Hysteresis	
U	Includes an internal termination pull-up resistor	
D	Includes an internal termination pull-down resistor	

**Table 2. Initialization Pin Functions**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
POSENSE	P22	VDD33	I <sub>4</sub> H	Async	Power-On Sense is an active high signal with hysteresis, that is generated from an external voltage monitor circuit. This signal should be driven active high when all the controller supply voltages have reached 90% of their specified minimum voltage. This signal should be driven inactive low after the falling edge of PWRGOOD as shown in <a href="#">Figure 2</a> Power Up and Power Down timing requirements. See also System Power-up sequence section.
PWRGOOD	T26	VDD33	I <sub>4</sub> H	Async	Power Good is an active high signal with hysteresis that is provided from an external voltage monitor circuit. A high value indicates all power is within operating voltage specifications and the system is safe to exit its RESET state. A transition from high to low is used to indicate that the DLPC900 and DMD supply voltage will drop below their rated minimum level. This transition must occur prior to the supply voltage drop as specified. During this interval, PONSENSE must remain active high. PWRGOOD serves as an early warning of an imminent power loss condition. A DMD park followed by a full controller reset is performed by the DLPC900 to protect the DMD. The minimum de-assertion time is used to protect the input from glitches. After the park sequence is complete, the DLPC900 will be held in its RESET state as long as PWRGOOD is low. PWRGOOD must be driven high for normal operation. The DLPC900 will acknowledge PWRGOOD as active once it's been driven high for its specified minimum time. See <a href="#">Figure 2</a> Power Up and Power Down timing requirements. See also System Power-up sequence section.

**Table 2. Initialization Pin Functions (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
EXT_ARSTZ	T24	VDD33	O <sub>2</sub>	Async	General purpose active low reset output signal. This output is driven low immediately after POSENSE is externally driven low, placing the system in RESET and remains low while POSENSE remains low. EXT_ARSTZ will continue to be held low after POSENSE is driven high and released by the controller firmware. EXT_ARSTZ is also driven low approximately 5us after the detection of a PWRGOOD or any internally generated reset. In all cases it will remain active for a minimum of 2 ms.
CTRL_ARSTZ	T25	VDD33	O <sub>2</sub>	Async	Controller active low reset output signal. This output is driven low immediately after POSENSE is externally driven low and remains low while POSENSE remains low. CTRL_ARSTZ will continue to be held low after POSENSE is driven high and released by the controller firmware. CTRL_ARSTZ is also optionally asserted low approximately 5us after the detection of a PWRGOOD or any internally generated reset. In all cases it will remain active for a minimum of 2 ms.

**Table 3. DMD Control Pin Functions**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION <sup>(1)</sup>
NAME	NUMBER				
DADOEZ	AE7	VDD33	O <sub>5</sub>	Async	DMD output-enable (active low). This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADADDR_3 DADADDR_2 DADADDR_1 DADADDR_0	AD6 AE5 AF4 AB8	VDD33	O <sub>5</sub>	Async	DMD address. This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADMODE_1 DADMODE_0	AD7 AE6	VDD33	O <sub>5</sub>	Async	DMD mode. This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADSEL_1 DADSEL_0	AE4 AC7	VDD33	O <sub>5</sub>	Async	DMD select. This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADSTRB	AF5	VDD33	O <sub>5</sub>	Async	DMD strobe. This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DAD_INTZ	AC8	VDD33	I <sub>4</sub> H	Async	DMD interrupt (active low). Requires an external 1-kΩ pull-up resistor.

(1) Refer to the [Typical Single Controller Chipset](#) and the [Typical Two Controller Chipset](#) for a description between a one controller and a two controller configuration.

**Table 4. DMD LVDS Interface Pin Functions<sup>(1)(2)</sup>**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
DCKA_P DCKA_N	V4 V3	VDD18	O <sub>7</sub>	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential clock
SCA_P SCA_N	V2 V1	VDD18	O <sub>7</sub>	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential serial control
DDA_P_15 DDA_N_15 DDA_P_14 DDA_N_14 DDA_P_13 DDA_N_13 DDA_P_12 DDA_N_12 DDA_P_11 DDA_N_11 DDA_P_10 DDA_N_10 DDA_P_9 DDA_N_9 DDA_P_8 DDA_N_8	P4 P3 P2 P1 R4 R3 R2 R1 T4 T3 T2 T1 U4 U3 U2 U1	VDD18	O <sub>7</sub>	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential serial data
DDA_P_7 DDA_N_7 DDA_P_6 DDA_N_6 DDA_P_5 DDA_N_5 DDA_P_4 DDA_N_4 DDA_P_3 DDA_N_3 DDA_P_2 DDA_N_2 DDA_P_1 DDA_N_1 DDA_P_0 DDA_N_0	W4 W3 W2 W1 Y2 Y1 Y4 Y3 AA2 AA1 AA4 AA3 AB2 AB1 AC2 AC1				
DCKB_P DCKB_N	J3 J4	VDD18	O <sub>7</sub>	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential clock
SCB_P SCB_N	J1 J2	VDD18	O <sub>7</sub>	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential serial control

(1) Several options allow reconfiguration of the DMD interface in order to better optimize board layout. The DLPC900 can swap channel A with channel B. The DLPC900 can also swap the data bit order within each channel independent of swapping the A and B channels.

(2) The DLPC900 is a full-bus DMD signaling interface. [Figure 16](#) shows the controller connections for this configuration.

**Table 4. DMD LVDS Interface Pin Functions<sup>(1)(2)</sup> (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
DDB_P_15	N1	VDD18	O <sub>7</sub>	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential serial data
DDB_N_15	N2				
DDB_P_14	N3				
DDB_N_14	N4				
DDB_P_13	M2				
DDB_N_13	M1				
DDB_P_12	M3				
DDB_N_12	M4				
DDB_P_11	L1				
DDB_N_11	L2				
DDB_P_10	L3				
DDB_N_10	L4				
DDB_P_9	K1				
DDB_N_9	K2				
DDB_P_8	K3				
DDB_N_8	K4				
DDB_P_7	H1				
DDB_N_7	H2				
DDB_P_6	H3				
DDB_N_6	H4				
DDB_P_5	G1				
DDB_N_5	G2				
DDB_P_4	G3				
DDB_N_4	G4				
DDB_P_3	F1				
DDB_N_3	F2				
DDB_P_2	F3				
DDB_N_2	F4				
DDB_P_1	E1				
DDB_N_1	E2				
DDB_P_0	D1				
DDB_N_0	D2				

**Table 5. Program Memory Flash Interface Pin Functions<sup>(1)</sup>**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION		
NAME	NUMBER				CHIP SELECT 0 (Additional Flash)	CHIP SELECT 1 (Boot Flash Only) <sup>(2)</sup>	CHIP SELECT 2 (Additional Flash)
PM_CSZ_0 <sup>(3)</sup>	D13	VDD33	O <sub>5</sub>	Async	Chip Select (active low)	N/A	N/A
PM_CSZ_1 <sup>(3)</sup>	E12	VDD33	O <sub>5</sub>	Async	N/A	Boot Flash Chip Select (active low)	N/A
PM_CSZ_2 <sup>(3)</sup>	A13	VDD33	O <sub>5</sub>	Async	N/A	N/A	Chip Select (active low)
PM_ADDR_22 <sup>(4)</sup>	A12	VDD33	B <sub>5</sub>	Async	Address bit (MSB)	Address bit (MSB)	Address bit (MSB)
PM_ADDR_21 <sup>(4)</sup>	E11	VDD33	B <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_20	D12	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_19	C12	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_18	B11	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_17	A11	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_16	D11	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit

(1) The default wait-state is set for a flash device of 120ns access time. Therefore, the slowest flash access time supported is 120ns. Refer to the [Program Memory Flash Interface](#) on how to program new wait-state values.

(2) Refer to the [Figure 23](#) for the memory layout of the boot flash.

(3) Requires an external 10-kΩ pull-up resistor.

(4) Requires an external 10-kΩ pull-down resistor.

**Table 5. Program Memory Flash Interface Pin Functions<sup>(1)</sup> (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION		
NAME	NUMBER				CHIP SELECT 0 (Additional Flash)	CHIP SELECT 1 (Boot Flash Only) <sup>(2)</sup>	CHIP SELECT 2 (Additional Flash)
PM_ADDR_15	C11	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_14	E10	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_13	D10	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_12	C10	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_11	B9	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_10	A9	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_9	E9	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_8	D9	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_7	C9	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_6	B8	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_5	A8	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_4	D8	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_3	C8	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_2	B7	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_1	A7	VDD33	O <sub>5</sub>	Async	Address bit	Address bit	Address bit
PM_ADDR_0	C7	VDD33	O <sub>5</sub>	Async	Address bit (LSB)	Address bit (LSB)	Address bit (LSB)
PM_WEZ	B12	VDD33	O <sub>5</sub>	Async	Write-Enable (active low)	Write-Enable (active low)	Write-Enable (active low)
PM_OEZ	C13	VDD33	O <sub>5</sub>	Async	Output-Enable (active low)	Output-Enable (active low)	Output-Enable (active low)
PM_BLSZ_1	B6	VDD33	O <sub>5</sub>	Async	UpperByte(15:8) Enable (active low)	N/A	UpperByte(15:8) Enable (active low)
PM_BLSZ_0	A6	VDD33	O <sub>5</sub>	Async	LowerByte(7:0) Enable (active low)	N/A	LowerByte(7:0) Enable (active low)
PM_DATA_15	C17	VDD33	B <sub>5</sub>	Async	Data bit (15)	Data bit (15)	Data bit (15)
PM_DATA_14	B16	VDD33	B <sub>5</sub>	Async	Data bit (14)	Data bit (14)	Data bit (14)
PM_DATA_13	A16	VDD33	B <sub>5</sub>	Async	Data bit (13)	Data bit (13)	Data bit (13)
PM_DATA_12	A15	VDD33	B <sub>5</sub>	Async	Data bit (12)	Data bit (12)	Data bit (12)
PM_DATA_11	B15	VDD33	B <sub>5</sub>	Async	Data bit (11)	Data bit (11)	Data bit (11)
PM_DATA_10	D16	VDD33	B <sub>5</sub>	Async	Data bit (10)	Data bit (10)	Data bit (10)
PM_DATA_9	C16	VDD33	B <sub>5</sub>	Async	Data bit (9)	Data bit (9)	Data bit (9)
PM_DATA_8	E14	VDD33	B <sub>5</sub>	Async	Data bit (8)	Data bit (8)	Data bit (8)
PM_DATA_7	D15	VDD33	B <sub>5</sub>	Async	Data bit (7)	Data bit (7)	Data bit (7)
PM_DATA_6	C15	VDD33	B <sub>5</sub>	Async	Data bit (6)	Data bit (6)	Data bit (6)
PM_DATA_5	B14	VDD33	B <sub>5</sub>	Async	Data bit (5)	Data bit (5)	Data bit (5)
PM_DATA_4	A14	VDD33	B <sub>5</sub>	Async	Data bit (4)	Data bit (4)	Data bit (4)
PM_DATA_3	E13	VDD33	B <sub>5</sub>	Async	Data bit (3)	Data bit (3)	Data bit (3)
PM_DATA_2	D14	VDD33	B <sub>5</sub>	Async	Data bit (2)	Data bit (2)	Data bit (2)
PM_DATA_1	C14	VDD33	B <sub>5</sub>	Async	Data bit (1)	Data bit (1)	Data bit (1)
PM_DATA_0	B13	VDD33	B <sub>5</sub>	Async	Data bit (0)	Data bit (0)	Data bit (0)



**Table 6. Port 1 and Port 2 Channel Data and Control Pin Functions<sup>(1)(2)(3)</sup>**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
P_CLK1	AE22	VDD33	I <sub>4</sub> D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated (Port 1 or Port 2 or (Port 1 and Port 2))).
P_CLK2	W25	VDD33	I <sub>4</sub> D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated (Port 1 or Port 2 or (Port 1 and Port 2))).
P_CLK3	AF23	VDD33	I <sub>4</sub> D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated (Port 1 or Port 2 or (Port 1 and Port 2))).
P_DATEN1	AF22	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Active high data enable. Selectable as to which port it is associated with (Port 1 or Port 2 or (Port 1 and Port 2)).
P_DATEN2	W24	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Active high data enable. Selectable as to which port it is associated with (Port 1 or Port 2 or (Port 1 and Port 2)).
P1_A9 P1_A8 P1_A7 P1_A6 P1_A5 P1_A4 P1_A3 P1_A2 P1_A1 P1_A0	AD15 AE15 AE14 AE13 AD13 AC13 AF14 AF13 AF12 AE12	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 1 A channel input pixel data (bit weight 128) Port 1 A channel input pixel data (bit weight 64) Port 1 A channel input pixel data (bit weight 32) Port 1 A channel input pixel data (bit weight 16) Port 1 A channel input pixel data (bit weight 8) Port 1 A channel input pixel data (bit weight 4) Port 1 A channel input pixel data (bit weight 2) Port 1 A channel input pixel data (bit weight 1) Port 1 A channel input pixel data (bit weight 0.5) Port 1 A channel input pixel data (bit weight 0.25)
P1_B9 P1_B8 P1_B7 P1_B6 P1_B5 P1_B4 P1_B3 P1_B2 P1_B1 P1_B0	AF18 AB18 AC15 AC16 AD16 AE16 AF16 AF15 AC14 AD14	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 1 B channel input pixel data (bit weight 128) Port 1 B channel input pixel data (bit weight 64) Port 1 B channel input pixel data (bit weight 32) Port 1 B channel input pixel data (bit weight 16) Port 1 B channel input pixel data (bit weight 8) Port 1 B channel input pixel data (bit weight 4) Port 1 B channel input pixel data (bit weight 2) Port 1 B channel input pixel data (bit weight 1) Port 1 B channel input pixel data (bit weight 0.5) Port 1 B channel input pixel data (bit weight 0.25)
P1_C9 P1_C8 P1_C7 P1_C6 P1_C5 P1_C4 P1_C3 P1_C2 P1_C1 P1_C0	AD20 AE20 AE21 AF21 AD19 AE19 AF19 AF20 AC19 AE18	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 1 C channel input pixel data (bit weight 128) Port 1 C channel input pixel data (bit weight 64) Port 1 C channel input pixel data (bit weight 32) Port 1 C channel input pixel data (bit weight 16) Port 1 C channel input pixel data (bit weight 8) Port 1 C channel input pixel data (bit weight 4) Port 1 C channel input pixel data (bit weight 2) Port 1 C channel input pixel data (bit weight 1) Port 1 C channel input pixel data (bit weight 0.5) Port 1 C channel input pixel data (bit weight 0.25)
P1_VSYNC	AC20	VDD33	B <sub>2</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 1 vertical sync. While intended to be associated with port 1, it can be programmed for use with port 2.
P1_HSYNC	AD21	VDD33	B <sub>2</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 1 horizontal sync. While intended to be associated with port 1, it can be programmed for use with port 2.

- (1) Ports 1 and 2 can be used separately as two 30-bit ports, or can be combined into one 60-bit port (typically, for high data rate sources) for transmission of two pixels per clock.
- (2) The A, B, C input data channels of ports 1 and 2 can be internally reconfigured or remapped for optimum board layout. Specifically each channel can individually remapped to the internal GBR/ YCbCr channels. For example, G data can be connected to channel A, B, or C and remapped to be appropriate channel internally. Port configuration and channel multiplexing is handled in the API software.
- (3) Sources feeding less than the full 10-bits per color component channel should be MSB justified when connected to the DLPC900 and the LSBs tied off to 0. For example, an 8-bit per color input should be connected to bits [9:2] of the corresponding A, B, C input channel. Three port clocks options (1,2,and 3) are provided to improve the signal integrity.

**Table 6. Port 1 and Port 2 Channel Data and Control Pin Functions<sup>(1)(2)(3)</sup> (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
P2_A9 P2_A8 P2_A7 P2_A6 P2_A5 P2_A4 P2_A3 P2_A2 P2_A1 P2_A0	AD26 AD25 AB21 AC22 AD23 AB20 AC21 AD22 AE23 AB19	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 2 A channel input pixel data (bit weight 128) Port 2 A channel input pixel data (bit weight 64) Port 2 A channel input pixel data (bit weight 32) Port 2 A channel input pixel data (bit weight 16) Port 2 A channel input pixel data (bit weight 8) Port 2 A channel input pixel data (bit weight 4) Port 2 A channel input pixel data (bit weight 2) Port 2 A channel input pixel data (bit weight 1) Port 2 A channel input pixel data (bit weight 0.5) Port 2 A channel input pixel data (bit weight 0.25)
P2_B9 P2_B8 P2_B7 P2_B6 P2_B5 P2_B4 P2_B3 P2_B2 P2_B1 P2_B0	Y22 AB26 AA23 AB25 AA22 AB24 AC26 AB23 AC25 AC24	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 2 B channel input pixel data (bit weight 128) Port 2 B channel input pixel data (bit weight 64) Port 2 B channel input pixel data (bit weight 32) Port 2 B channel input pixel data (bit weight 16) Port 2 B channel input pixel data (bit weight 8) Port 2 B channel input pixel data (bit weight 4) Port 2 B channel input pixel data (bit weight 2) Port 2 B channel input pixel data (bit weight 1) Port 2 B channel input pixel data (bit weight 0.5) Port 2 B channel input pixel data (bit weight 0.25)
P2_C9 P2_C8 P2_C7 P2_C6 P2_C5 P2_C4 P2_C3 P2_C2 P2_C1 P2_C0	W23 V22 Y26 Y25 Y24 Y23 W22 AA26 AA25 AA24	VDD33	I <sub>4</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 2 C channel input pixel data (bit weight 128) Port 2 C channel input pixel data (bit weight 64) Port 2 C channel input pixel data (bit weight 32) Port 2 C channel input pixel data (bit weight 16) Port 2 C channel input pixel data (bit weight 8) Port 2 C channel input pixel data (bit weight 4) Port 2 C channel input pixel data (bit weight 2) Port 2 C channel input pixel data (bit weight 1) Port 2 C channel input pixel data (bit weight 0.5) Port 2 C channel input pixel data (bit weight 0.25)
P2_VSYNC	U22	VDD33	B <sub>2</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 2 vertical sync. While intended to be associated with port 2, it can be programmed for use with port 1.
P2_HSYNC	W26	VDD33	B <sub>2</sub> D	P_CLK1, P_CLK2, or, P_CLK3	Port 2 horizontal sync. While intended to be associated with port 2, it can be programmed for use with port 1.

**Table 7. Clock and PLL Support Pin Functions**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
MOSC	M26	VDD33	I <sub>10</sub>	N/A	System clock oscillator input (3.3-V LVTTTL). MOSC must be stable a maximum of 25 ms after POSENSE transitions from low to high.
MOSCN	N26	VDD33	O <sub>10</sub>	N/A	MOSC crystal return.
OCLKA <sup>(1)</sup>	AF6	VDD33	O <sub>5</sub>	Async	General-purpose output clock A. The frequency is software programmable. Power-up default is 787 kHz and the output frequency is maintained through all operations, except power loss and reset.

- (1) This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected. Refer to the [Typical Single Controller Chipset](#) and the [Typical Two Controller Chipset](#) for a description between a one controller and a two controller configuration.

**Table 8. Board Level Test and Debug Pin Functions<sup>(1)</sup>**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
TDI	N25	VDD33	I <sub>4</sub> U	TCK	JTAG serial data in. Used in both Boundary Scan and ICE modes.

- (1) All JTAG signals are LVTTTL compatible.

**Table 8. Board Level Test and Debug Pin Functions<sup>(1)</sup> (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
TCK	N24	VDD33	I <sub>4</sub> D	N/A	JTAG serial data clock. Used in both Boundary Scan and ICE modes.
TMS1	P25	VDD33	I <sub>4</sub> U	TCK	JTAG test mode select. Used in Boundary Scan mode.
TMS2	P26	VDD33	I <sub>4</sub> U	TCK	JTAG-ICE test mode select. Used in ICE mode.
TDO1	N23	VDD33	O <sub>5</sub>	TCK	JTAG serial data out. Used in Boundary Scan mode.
TDO2	N22	VDD33	O <sub>5</sub>	TCK	JTAG-ICE serial data out. Used in ICE mode.
TRSTZ	M23	VDD33	I <sub>4</sub> H U	Async	JTAG Reset. Used in both Boundary Scan and ICE modes. This pin should be pulled high (or left unconnected) when the JTAG interface is in use for boundary scan or debug. Connect this to ground otherwise. Failure to tie this pin low during normal operation will cause startup and initialization problems.
RTCK	E4	VDD33	O <sub>2</sub>	N/A	JTAG return clock. Used in ICE mode.
ICTSEN	M24	VDD33	I <sub>4</sub> H D	Async	IC tri-state enable (active high). Asserting high will tri-state all outputs except the JTAG interface. Requires an external 4.7 kΩ pull-down resistor.

**Table 9. Device Test Pin Functions**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
HW_TEST_EN	M25	VDD33	I <sub>4</sub> H D	N/A	Device manufacturing test enable. This signal must be connected to an external ground for normal operation.

**Table 10. Peripheral Interface Pin Functions**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
I2C0_SCL	A10	VDD33	B <sub>8</sub>	N/A	I <sup>2</sup> C Bus 0, Clock. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pull-up resistor to 3.3 V. The minimum acceptable pull-up value is 1 kΩ resistor.
I2C0_SDA	B10	VDD33	B <sub>8</sub>	I2C0_SCL	I <sup>2</sup> C Bus 0, Data. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pull-up resistor to 3.3 V. The minimum acceptable pull-up value is 1 kΩ resistor.
I2C1_SDA <sup>(1)</sup>	E19	VDD33	B <sub>2</sub>	I2C1_SCL	I <sup>2</sup> C Bus 1, Data. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pull-up resistor to 3.3 V. The minimum acceptable pull-up value is 1 kΩ resistor.
I2C1_SCL <sup>(1)</sup>	D20	VDD33	B <sub>2</sub>	N/A	I <sup>2</sup> C Bus 1, Clock. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pull-up resistor to 3.3 V. The minimum acceptable pull-up value is 1 kΩ resistor.
I2C2_SDA <sup>(1)</sup>	C21	VDD33	B <sub>2</sub>	I2C2_SCL	I <sup>2</sup> C Bus 2, Data. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pull-up resistor to 3.3 V. The minimum acceptable pull-up value is 1 kΩ resistor.
I2C2_SCL <sup>(1)</sup>	B22	VDD33	B <sub>2</sub>	N/A	I <sup>2</sup> C Bus 2, Clock. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pull-up resistor to 3.3 V. The minimum acceptable pull-up value is 1 kΩ resistor.

(1) This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected. Refer to the [Typical Single Controller Chipset](#) and the [Typical Two Controller Chipset](#) for a description between a one controller and a two controller configuration.

**Table 10. Peripheral Interface Pin Functions (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
SSP0_CLK	AD4	VDD33	B <sub>5</sub>	N/A	Synchronous serial port 0, clock
SSP0_RXD	AD5	VDD33	I <sub>4</sub>	SSP0_CLK	Synchronous serial port 0, Receive Data In
SSP0_TXD	AB7	VDD33	O <sub>5</sub>	SSP0_CLK	Synchronous serial port 0, Transmit Data Out
SSP0_CSZ_0 <sup>(1)</sup>	AC5	VDD33	B <sub>5</sub>	SSP0_CLK	Synchronous serial port 0, chip select 0 (active low)
SSP0_CSZ_1 <sup>(1)</sup>	AB6	VDD33	B <sub>5</sub>	SSP0_CLK	Synchronous serial port 0, chip select 1 (active low)
SSP0_CSZ_2 <sup>(1)</sup>	AC3	VDD33	B <sub>5</sub>	SSP0_CLK	Synchronous serial port 0, chip select 2 (active low)
UART0_TXD	AB3	VDD33	O <sub>5</sub>	Async	UART0, UART transmit data output. The firmware only outputs debug messages on this port.
UART0_RXD	AD1	VDD33	I <sub>4</sub>	Async	UART0, UART receive data input. The firmware does not support receiving data on this port.
UART0_RTSZ	AD2	VDD33	O <sub>5</sub>	Async	UART0, UART ready to send hardware flow control output (active low)
UART0_CTSZ	AE2	VDD33	I <sub>4</sub>	Async	UART0, UART clear to send hardware flow control input (active low). This pin equires an external 10 kΩ pull-down resister.
USB_DAT_N <sup>(1)</sup> USB_DAT_P	C5 D6	VDD33	B <sub>9</sub>	Async	USB D– I/O USB D+ I/O
HOLD_BOOTZ	F24	VDD33	B <sub>2</sub>	Async	Boot mode. When this pin is held low, the firmware boots-up in bootload mode. When pin is held high, the firmware boots-up in normal operating mode. This pin requires an external 1 kΩ pull-up resister.
USB_ENZ <sup>(1)</sup>	E25	VDD33	B <sub>2</sub>	Async	The firmware will use this pin to enable an external buffer on the USB data lines after it has completed initialization.
FAULT_STATUS	AC11	VDD33	O <sub>2</sub>	Async	This signal toggles or held high to indicate status faults.
HEARTBEAT	AB12	VDD33	O <sub>2</sub>	Async	This signal toggles to indicate the system is operational. Period is ~1second.
SEQ_INT2	H26	VDD33	I <sub>2</sub>	Async	This signal servers as an interrupt for pattern sequencing and must be connected to SEQ_AUX6.
SEQ_INT1	G26	VDD33	I <sub>2</sub>	Async	This signal servers as an interrupt for pattern sequencing and must be connected to SEQ_AUX7.
SEQ_AUX7	F26	VDD33	O <sub>2</sub>	Async	This signal servers as an interrupt for pattern sequencing and must be connected to SEQ_INT1.
SEQ_AUX6	E26	VDD33	O <sub>2</sub>	Async	This signal servers as an interrupt for pattern sequencing and must be connected to SEQ_INT2.
TEST_FUNC_5 <sup>(1)</sup>	K22	VDD33	B <sub>2</sub>	Async	On DLP® LightCrafter 9000 EVM, this pin connects to FPGA and could server as a configuration pin. Otherwise can be left unconnected.
TEST_FUNC_4 <sup>(1)</sup>	J26	VDD33	B <sub>2</sub>	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and could server as a configuration pin. Otherwise can be left unconnected.
TEST_FUNC_3 <sup>(1)</sup>	J25	VDD33	B <sub>2</sub>	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and servers as a configuration pin. This function configures the 24-bit parallel data output of the FPGA to be split between the master and the slave controllers. The firmware will set this pin high by default.
TEST_FUNC_2 <sup>(1)</sup>	J24	VDD33	B <sub>2</sub>	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and could server as a configuration pin. Otherwise can be left unconnected.
TEST_FUNC_1 <sup>(1)</sup>	J23	VDD33	B <sub>2</sub>	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and could server as a configuration pin. Otherwise can be left unconnected.

**Table 10. Peripheral Interface Pin Functions (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
GPIO_08 <sup>(1)</sup>	E21	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 8. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_07 <sup>(1)</sup>	V23	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 7. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_06 <sup>(1)</sup>	V24	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 6. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_05 <sup>(1)</sup>	U24	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 5. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_04 <sup>(1)</sup>	U25	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 4. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_PWM_03 <sup>(1)</sup>	A23	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 3 or PWM 3. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_PWM_02 <sup>(1)</sup>	A22	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 2 or PWM 2. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_PWM_01 <sup>(1)</sup>	B21	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 1 or PWM 1. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>
GPIO_PWM_00 <sup>(1)</sup>	A21	VDD33	B <sub>2</sub>	Async	This pin can be configured as GPIO 0 or PWM 0. An external pull-up resistor is required when this pin is configured as open-drain. <sup>(2)</sup>

- (2) GPIO signals must be configured through software for input, output, bidirectional, or open-drain. Some GPIO have one or more alternative use modes, which are also software configurable. The reset default for all GPIO signals is as an input signal. Refer to the DLPC900 Programmers Guide.

**Table 11. Trigger Control Pin Functions**

Pin <sup>(1)</sup>		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
TRIG_IN_1	AF7	VDD33	I <sub>4</sub>	Async	In video pattern mode, this signal is used for advancing the pattern display.
TRIG_IN_2	H25	VDD33	I <sub>2</sub>	Async	In video pattern mode, the rising edge of this signal is used for starting the pattern display and the falling edge is used for stopping the pattern display. It works along with the software start stop command.
TRIG_OUT_1	E20	VDD33	O <sub>2</sub>	Async	Active high trigger output signal during pattern exposure.
TRIG_OUT_2	D22	VDD33	O <sub>2</sub>	Async	Active high trigger output to indicate first pattern display.

- (1) These signals do not apply to the slave controller in a two controller system configuration. On the slave controller, these pins are reserved and should be left unconnected. Refer to the [Typical Single Controller Chipset](#) and the [Typical Two Controller Chipset](#) for a description between a one controller and a two controller configuration.

**Table 12. LED Control Pin Functions**

Pin <sup>(1)</sup>		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
BLU_LED_PWM	C20	VDD33	O <sub>2</sub>	Async	Blue LED PWM current control signal
GRN_LED_PWM	B20	VDD33	O <sub>2</sub>	Async	Green LED PWM current control signal
RED_LED_PWM	B19	VDD33	O <sub>2</sub>	Async	Red LED PWM current control signal

- (1) These signals do not apply to the slave controller in a two controller system configuration. On the slave controller, these pins are reserved and should be left unconnected. Refer to the [Typical Single Controller Chipset](#) and the [Typical Two Controller Chipset](#) for a description between a one controller and a two controller configuration.

**Table 12. LED Control Pin Functions (continued)**

Pin <sup>(1)</sup>		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
BLU_LED_EN	D24	VDD33	O <sub>2</sub>	Async	Blue LED enable signal.
GRN_LED_EN	C25	VDD33	O <sub>2</sub>	Async	Green LED enable signal.
RED_LED_EN	B26	VDD33	O <sub>2</sub>	Async	Red LED enable signal.

**Table 13. Two Controller Support Pin Functions**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION <sup>(1)</sup>
NAME	NUMBER				
SEQ_SYNC	AB9	VDD33	B <sub>3</sub>	Async	Sequence sync. This signal must be connected between the master and slave controller in a two controller configuration. Do not leave unconnected. This pin requires an external 10-kΩ pull-up resistor.
SSP0_CSZ4_SLV	U26	VDD33	B <sub>2</sub>	SSP0_CLK	This signal is used by the master controller to communicate with the slave controller over the SSP interface. This pin requires an external 4.7-kΩ pull-up resistor
FSD12_OUTPUT	T23	VDD33	B <sub>2</sub>	Async	This pin must be connected to DA_SYNC_INPUT <sup>(2)</sup>
DA_SYNC_INPUT	R22	VDD33	B <sub>2</sub>	Async	This pin must be connected to FSD12_OUTPUT <sup>(3)</sup>
SLV_CTRL_PRST	V25	VDD33	B <sub>2</sub>	Async	This signal must be connected between the master and slave controller in a two controller configuration. The slave controller will pull this signal high to inform the master controller that it is present and ready. This pin requires an external 10-kΩ pull-down resistor. Do not leave unconnected.
CTRL_MODE_CFG	V26	VDD33	B <sub>2</sub>	Async	When this pin is high, the controller operates as the master controller. When this pin is low the controller operates as the slave controller. Use an external 4.7-kΩ pull-up or pull-down resistor to identify the controller. Do not leave unconnected.

(1) Refer to the [Typical Single Controller Chipset](#) and the [Typical Two Controller Chipset](#) for a description between a one controller and a two controller configuration.

(2) The FSD12\_OUTPUT of the slave controller must be left unconnected.

(3) The DA\_SYNC\_INPUT of the slave controller must be connected to the FSD12\_OUTPUT of the master controller.

**Table 14. Reserved Pin Functions**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
AFE_ARSTZ	AC12	VDD33	O <sub>2</sub>	Async	Reserved. This pin requires an external 4.7-kΩ pull-up resistor.
RESERVED_AD12	AD12	VDD33	O <sub>6</sub>	N/A	Reserved. Should be left unconnected.
AFE_IRQ	AB13	VDD33	I <sub>4</sub>	Async	Reserved. Should be left unconnected.
RESERVED_AF11	AF11	VDD33	I <sub>4</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AD11	AD11	VDD33	I <sub>4</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AE11	AE11	VDD33	I <sub>4</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AE8	AE8	VDD33	I <sub>4</sub>	N/A	Reserved. This pin requires an external 10-kΩ pull-up resistor.
RESERVED_AD8	AD8	VDD33	O <sub>5</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AC9	AC9	VDD33	O <sub>5</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AF8	AF8	VDD33	I <sub>4</sub>	N/A	Reserved. This pin Requires an external 10-kΩ pull-down resistor.
RESERVED_E3	E3	VDD33	B <sub>5</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AB10	AB10	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AD9	AD9	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AE9	AE9	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AF9	AF9	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AB11	AB11	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.



**Table 14. Reserved Pin Functions (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
RESERVED_AC10	AC10	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AD10	AD10	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AE10	AE10	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AF10	AF10	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_K24	K24	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_K23	K23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_J22	J22	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_H24	H24	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_H23	H23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_H22	H22	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_G25	G25	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_F25	F25	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_G24	G24	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_G23	G23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_T22	T22	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_U23	U23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_G22	G22	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_F23	F23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_D26	D26	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_E24	E24	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_F22	F22	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_D25	D25	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_E23	E23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_C26	C26	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_AB4	AB4	VDD33	B <sub>5</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_C23	C23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_D21	D21	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_B24	B24	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_C22	C22	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_B23	B23	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_A20	A20	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_A19	A19	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_E18	E18	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_D19	D19	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_C19	C19	VDD33	B <sub>2</sub>	N/A	Reserved. Should be left unconnected.
RESERVED_E8	E8	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_B4	B4	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_C4	C4	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_E7	E7	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_D5	D5	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_E6	E6	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.

**Table 14. Reserved Pin Functions (continued)**

Pin		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
RESERVED_D3	D3	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_C2	C2	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_A4	A4	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_B5	B5	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_C6	C6	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_A5	A5	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.
RESERVED_D7	D7	VDD33	B <sub>2</sub> D	N/A	Reserved. Should be left unconnected.

**Table 15. Power and Ground Pin Functions**

Pin		I/O TYPE	DESCRIPTION
NAME	NUMBER		
VDD33	F20, F17, F11, F8, L21, R21, Y21, AA19, AA16, AA10, AA7	PWR	3.3-V I/O power
VDD18	C1, F5, G6, K6, M5, P5, T5, W6, AA5, AE1 H5, N6, T6, AA13, U21, P21, H21, F14	PWR	1.8-V internal DRAMVDD and LVDSAVD I/O power (To shut this power down in a system low-power mode, see the <a href="#">System Power-Up Sequence</a> .)
VDDC	F19, F16, F13, F10, F7, H6, L6, P6, U6, Y6, AA8, AA11, AA14, AA17, AA20, W21, T21, N21, K21, G21, L11, T11, T16, L16	PWR	1.15-V core power
PLLD_VDD	L22	PWR	1.15-V DMD clock generator PLL Digital power
PLLD_VSS	L23	GND	1.15-V DMD clock generator PLL Digital GND
PLLD_VAD	K25	PWR	1.8-V DMD clock generator PLL Analog power
PLLD_VAS	K26	GND	1.8-V DMD clock generator PLL Analog GND
PLLM1_VDD	L26	PWR	1.15-V master-LS clock generator PLL Digital power
PLLM1_VSS	M22	GND	1.15-V master-LS clock generator PLL Digital GND
PLLM1_VAD	L24	PWR	1.8-V master-LS clock generator PLL Analog power
PLLM1_VAS	L25	GND	1.8-V master-LS clock generator PLL Analog GND
PLLM2_VDD	P23	PWR	1.15-V master-HS clock generator PLL Digital power
PLLM2_VSS	P24	GND	1.15-V master-HS clock generator PLL Digital GND
PLLM2_VAD	R25	PWR	1.8-V master-HS clock generator PLL Analog power
PLLM2_VAS	R26	GND	1.8-V master-HS clock generator PLL Analog GND
PLLS_VAD	R23	PWR	1.15-V video-2X clock generator PLL Analog power
PLLS_VAS	R24	GND	1.15-V video-2X clock generator PLL Analog GND



**Table 15. Power and Ground Pin Functions (continued)**

Pin		I/O TYPE	DESCRIPTION
NAME	NUMBER		
L_VDQPAD_[7:0], R_VDQPAD_[7:0]	B18, D18, B17, E17, A18, C18, A17, D17, AE17, AC17, AF17, AC18, AB16, AD17, AB17, AD18	RES	DRAM direct test pins (for manufacturing use only). These pins should be tied directly to ground for normal operation.
CFO_VDD33	AE26	RES	DRAM direct test control pin (for manufacturing use only). This pin should be tied directly to 3.3 I/O power (VDD33) for normal operation.
VTEST1, VTEST2, VTEST3, VTEST4	AB14, AB15, E15, E16	RES	DRAM direct test control pins (for manufacturing use only). These pins should be tied directly to ground for normal operation.
LVDS_AVS1, LVDS_AVS2	V5, K5	PWR	Dedicated ground for LVDS bandgap reference. These pins should be tied directly to ground for normal operation.
VPGM	AC6	PWR	Fuse programming pin (for manufacturing use only). This pin should be tied directly to ground for normal operation.
GND	A26, A25, A24, B25, C24, D23, E22, F21, F18, F15, F12, F9, F6, E5, D4, C3, B3, A3, B2, A2, B1, A1, G5, J5, J6, L5, M6, N5, R5, R6, U5, V6, W5, Y5, AA6, AB5, AC4, AD3, AE3, AF3, AF2, AF1, AA9, AA12, AA15, AA18, AA21, AB22, AC23, AD24, AE24, AF24, AE25, AF25, AF26, V21, M21, J21, L15, L14, L13, L12, M16, M15, M14, M13, M12, M11, N16, N15, N14, N13, N12, N11, P16, P15, P14, P13, P12, P11, R16, R15, R14, R13, R12, R11, T15, T14, T13, T12	GND	Common ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Supply voltage <sup>(2)(3)</sup>	VDDC (core)	−0.3	1.6	V
	VDD18 (LVDS/AVD I/O and internal DRAMVDD)	−0.3	2.5	
	VDD33 (I/O)	−0.3	3.9	
	PLLD_VDD (1.15 V DMD clock generator – digital)	−0.3	1.6	
	PLLM1_VDD (1.15 V master-LS clock generator – digital)	−0.3	1.6	
	PLLM2_VDD (1.15 V master-HS clock generator – digital)	−0.3	1.6	
	PLLD_VAD (1.8 V DMD clock generator – analog)	−0.3	2.5	
	PLLM1_VAD (1.8 V master-LS clock generator – analog)	−0.3	2.5	
	PLLM2_VAD (1.8 V master-HS clock generator – analog)	−0.3	2.5	
	PLLS_VAD (1.15 V video-2X – analog)	−0.5	1.4	
Input voltage, V <sub>I</sub> <sup>(4)</sup>	USB	−1	5.25	V
	OSC	−0.3	VDD33 + 0.3 V	
	3.3 LVTTTL	−0.3	3.6	
	3.3 I <sup>2</sup> C	−0.5	3.8	
Output voltage, V <sub>O</sub>	USB	−1	5.25	V
	1.8 LVDS	−0.3	2.2	
	3.3 LVTTTL	−0.3	3.6	
	3.3 I <sup>2</sup> C	−0.5	3.8	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) All of the 3.3-, 1.8-, and 1.15 V power should be applied and removed per the procedure defined in the [System Power-Up Sequence](#). Overlap currents, if allowed to continue flowing unchecked not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.
- (4) Applies to external input and bidirectional buffers.

### 6.2 Handling Ratings

			MIN	MAX	UNIT
T <sub>J</sub>	Operating junction temperature range		0	111	°C
T <sub>stg</sub>	Storage temperature range		−40	125	
V <sub>(ESD)</sub> <sup>(1)</sup>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(2)</sup>	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(3)</sup>	−300	+500	
		ESD sensitivity machine model (MM)	−200	+200	

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		I/O <sup>(1)</sup>	MIN	NOM	MAX	UNIT
V <sub>DD33</sub>	3.3 V supply voltage, I/O		3.135	3.3	3.465	V
V <sub>DD18</sub>	1.8 V supply voltage, LVDSAVD and DRAMVDD		1.71	1.8	1.89	
V <sub>DDC</sub>	1.15 V supply voltage, Core logic		1.100	1.15	1.200	
PLLD_V <sub>DD</sub>	1.8 V supply voltage, PLL analog		1.71	1.8	1.89	
PLLM1_V <sub>DD</sub>	1.8 V supply voltage, PLL analog		1.71	1.8	1.89	
PLLM2_V <sub>DD</sub>	1.8 V supply voltage, PLL analog		1.71	1.8	1.89	
PLLS_V <sub>DD</sub>	1.15 V supply voltage, PLL analog		1.090	1.15	1.200	
PLLD_V <sub>DD</sub>	1.15 V supply voltage, PLL digital		1.090	1.15	1.200	
PLLM1_V <sub>DD</sub>	1.15 V supply voltage, PLL digital		1.090	1.15	1.200	
PLLM2_V <sub>DD</sub>	1.15 V supply voltage, PLL digital		1.090	1.15	1.200	
V <sub>I</sub>	Input voltage	USB (9)	0		V <sub>DD33</sub>	V
		OSC (10)	0		V <sub>DD33</sub>	
		3.3 V LVTTTL (1, 2, 3, 4)	0		V <sub>DD33</sub>	
		3.3 V I <sup>2</sup> C (8)	0		V <sub>DD33</sub>	
V <sub>O</sub>	Output voltage	USB (8)	0		V <sub>DD33</sub>	V
		3.3 V LVTTTL (1, 2, 3, 4)	0		V <sub>DD33</sub>	
		3.3 V I <sup>2</sup> C (8)	0		V <sub>DD33</sub>	
		1.8 V LVDS (7)	0		V <sub>DD18</sub>	
T <sub>A</sub>	Operating ambient temperature range	See <sup>(2)</sup> and <sup>(3)</sup>	0		55	°C
T <sub>C</sub>	Operating top-center case temperature	See <sup>(3)</sup> and <sup>(4)</sup>	0		109.16	°C
T <sub>J</sub>	Operating junction temperature		0		111	°C

(1) The number inside the parentheses for the I/O refers to the I/O type defined in [Table 1](#).

(2) Assumes minimum 1 m/s airflow.

(3) Maximum thermal values assume max power of 4.76 W (total for controller).

(4) Assume  $\phi_{JT}$  equals 0.4 °C/W.

### 6.4 Thermal Information

THERMAL METRIC		DLPC900	UNIT
		BGA (516 Pins)	
R <sub>θJC</sub> <sup>(1)</sup>	Junction-to-Air Thermal resistance	4.4	°C/W
R <sub>θJA</sub> at 0 m/s of forced airflow <sup>(2)</sup>	Junction-to-Air Thermal resistance	14.4	
R <sub>θJA</sub> at 1 m/s of forced airflow <sup>(2)</sup>	Junction-to-Air Thermal resistance	9.5	
R <sub>θJA</sub> at 2 m/s of forced airflow <sup>(2)</sup>	Junction-to-Air Thermal resistance	9.0	
φ <sub>JT</sub> <sup>(3)</sup>	Temperature variance from junction to package top center temperature, per unit power dissipation	0.4	

(1) R<sub>θJC</sub> analysis assumptions: The heat generated in the chip flows into overmold (top side) and also into the package laminate (bottom side) and then into PCB via package solder balls. Should be used for heat sink analysis only.

(2) Thermal coefficients abide by JEDEC Standard 51. R<sub>θJA</sub> is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC900 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.

(3) Example: (3.2 W) × (0.4 C/W) ≈ 1.28°C temperature rise.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>			TEST CONDITIONS <sup>(2)</sup>	MIN	NOM	MAX	UNIT
V <sub>IH</sub>	High-level input threshold voltage	USB (9)		2			V
		OSC (10)		2			
		3.3-V LVTTL (1, 2, 3, 4)		2			
		3.3-V I <sup>2</sup> C (8)		2.4	VDD33 + 0.5		
V <sub>IL</sub>	Low-level input threshold voltage	USB (9)				0.8	V
		OSC (10)				0.8	
		3.3-V LVTTL (1, 2, 3, 4)				0.8	
		3.3-V I <sup>2</sup> C (8)		–0.5		1	
V <sub>DIS</sub>	Differential input sensitivity (Differential input voltage)	USB (9)		200			mV
V <sub>ICM</sub>	Input common mode range (Differential cross point voltage)	USB (9)		0.8		2.5	V
V <sub>OH</sub>	High-level output voltage	USB (9)		2.8			V
		1.8-V LVDS (7)		1.52			
		3.3-V LVTTL (1, 2, 3)	I <sub>OH</sub> = Max rated	2.7			
V <sub>OL</sub>	Low-level output voltage	USB (9)		0		0.3	V
		1.8-V LVDS (7)				0.88	
		3.3-V LVTTL (1, 2, 3)	I <sub>OL</sub> = Max rated			0.4	
		3.3-V I <sup>2</sup> C (8)	I <sub>OL</sub> = 3-mA sink			0.4	
V <sub>OD</sub>	Output differential voltage	1.8-V LVDS (7)		0.065		0.44	V
I <sub>IH</sub>	High-level input current	USB (9)				200	μA
		OSC (10)		–10		10	
		3.3-V LVTTL (1 to 4) (without internal pull-down)	V <sub>IH</sub> = VDD33	–10		10	
		3.3-V LVTTL (1 to 4) (with internal pull-down)	V <sub>IH</sub> = VDD33	10		200	
		3.3-V I <sup>2</sup> C (8)	V <sub>IH</sub> = VDD33			10	
I <sub>IL</sub>	Low-level input current	USB (9)		–10		10	μA
		OSC (10)		–10		10	
		3.3-V LVTTL (1-4) (without internal pull-up)	V <sub>OH</sub> = VDD33	–10		10	
		3.3-V LVTTL (1-4) (with internal pull-up)	V <sub>OH</sub> = VDD33	–10		–200	
		3.3-V I <sup>2</sup> C (8)	V <sub>OH</sub> = VDD33			–10	

(1) The number inside the parentheses for the I/O refers to the I/O type defined in [Table 1](#).

(2) Normal mode refers to DLPC900 operation during full functionality. Typical values correspond to power dissipated on nominal process devices operating at nominal voltage and 70°C junction temperature (approximately 25°C ambient) displaying typical video-graphics content from a high-frequency source. Max values correspond to power dissipated on fast-process devices operating at high voltage and 105°C junction temperature (approximately 55°C ambient) displaying typical video-graphics content from a high-frequency source. The increased power dissipation observed on fast-process devices operated at max recommended temperature is primarily a result of increased leakage current.

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>			TEST CONDITIONS <sup>(2)</sup>	MIN	NOM	MAX	UNIT
$I_{OH}$	High-level output current <sup>(3)</sup>	USB (9)		–18.4			mA
		1.8-V LVDS (7) ( $V_{OD} = 300$ mV)	$V_O = 1.4$ V	–6.5			
		3.3-V LVTTL (1)	$V_O = 2.4$ V	–4			
		3.3-V LVTTL (2)	$V_O = 2.4$ V	–8			
		3.3-V LVTTL (3)	$V_O = 2.4$ V	–12			
$I_{OL}$	Low-level output current <sup>(4)</sup>	USB (9)		19.1			mA
		1.8-V LVDS (7) ( $V_{OD} = 300$ mV)	$V_O = 1$ V	6.5			
		3.3-V LVTTL (1)	$V_O = 0.4$ V	4			
		3.3-V LVTTL (2)	$V_O = 0.4$ V	8			
		3.3-V LVTTL (3)	$V_O = 0.4$ V	12			
		3.3-V I <sup>2</sup> C (8)		3			
$I_{OZ}$	High-impedance leakage current	USB (9)		–10		10	$\mu$ A
		LVDS (7)		–10		10	
		3.3-V LVTTL (1, 2, 3)		–10		10	
		3.3-V I <sup>2</sup> C (8)		–10		10	
$C_i$	Input capacitance (including package)	USB (9)		11.84		17.07	pF
		3.3-V LVTTL (1)		3.75		5.52	
		3.3-V LVTTL (2)		3.75		5.52	
		3.3-V LVTTL (4)		3.75		5.52	
		3.3-V I <sup>2</sup> C (8)		5.26		6.54	

(3)  $V_{DDQ} = 1.7$  V;  $V_{OUT} = 1420$  mV.  $(V_{OUT} - V_{DDQ}) / I_{OH}$  must be  $< 21 \Omega$  for values of  $V_{OUT}$  between  $V_{DDQ}$  and  $V_{DDQ} - 280$  mV.

(4)  $V_{DDQ} = 1.7$  V;  $V_{OUT} = 280$  mV.  $V_{OUT} / I_{OL}$  must be  $< 21 \Omega$  for values of  $V_{OUT}$  between 0 V and 280 mV.

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

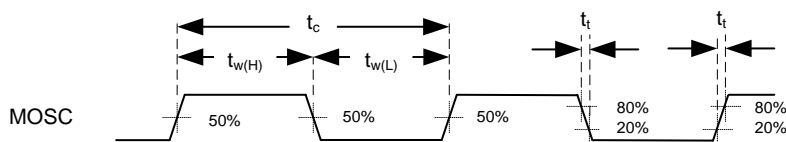
PARAMETER <sup>(1)</sup>		TEST CONDITIONS <sup>(2)</sup>	MIN	NOM	MAX	UNIT
I <sub>CC11</sub>	Supply voltage, 1.15-V core power	Normal mode			2368	mA
I <sub>CC18</sub>	Supply voltage, 1.8-V power (LVDS I/O and internal DRAM)	Normal mode			1005	mA
I <sub>CC33</sub>	Supply voltage, 3.3-V I/O power	Normal mode			33	mA
I <sub>CC11_PLLD</sub>	Supply voltage, DMD PLL digital power (1.15 V)	Normal mode		4.4	6.2	mA
I <sub>CC11_PLLM1</sub>	Supply voltage, master-LS clock generator PLL digital power (1.15 V)	Normal mode		4.4	6.2	mA
I <sub>CC11_PLLM2</sub>	Supply voltage, master-HS clock generator PLL digital power (1.15 V)	Normal mode		4.4	6.2	mA
I <sub>CC18_PLLD</sub>	Supply voltage, DMD PLL analog power (1.8 V)	Normal mode		8	10.2	mA
I <sub>CC18_PLLM1</sub>	Supply voltage, master-LS clock generator PLL analog power (1.8 V)	Normal mode		8	10.2	mA
I <sub>CC18_PLLM2</sub>	Supply voltage, master-HS clock generator PLL analog power (1.8 V)	Normal mode		8	10.2	mA
I <sub>CC11_PLLS</sub>	Supply voltage, video-2X PLL analog power (1.15 V)	Normal mode			2.9	mA
<b>Total Power in Normal Mode</b>					4.76	W

## 6.6 System Oscillators Timing Requirements<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency, MOSC1 Stability and Tolerance. Crystal frequency 20MHz. <sup>(2)</sup>		19.998 100	20.002 100	MHz ppm
$t_c$	Cycle time, MOSC1		49.995	50.005	ns
$t_{w(H)}$	Pulse duration2, MOSC, high	50% to 50% reference points (signal)	20		ns
$t_{w(L)}$	Pulse duration2, MOSC, low	50% to 50% reference points (signal)	20		ns
$t_t$	Transition time2, MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)		12	ns
$t_{jp}$	Period jitter2, MOSC (The deviation in period from ideal period due solely to high-frequency jitter – not spread spectrum clocking)			18	ps

(1) Applies only when driven through an external digital oscillator. The MOSC input cannot support spread spectrum clock spreading.

(2) Including impact to accuracy due to aging, temperature, and trim sensitivity.

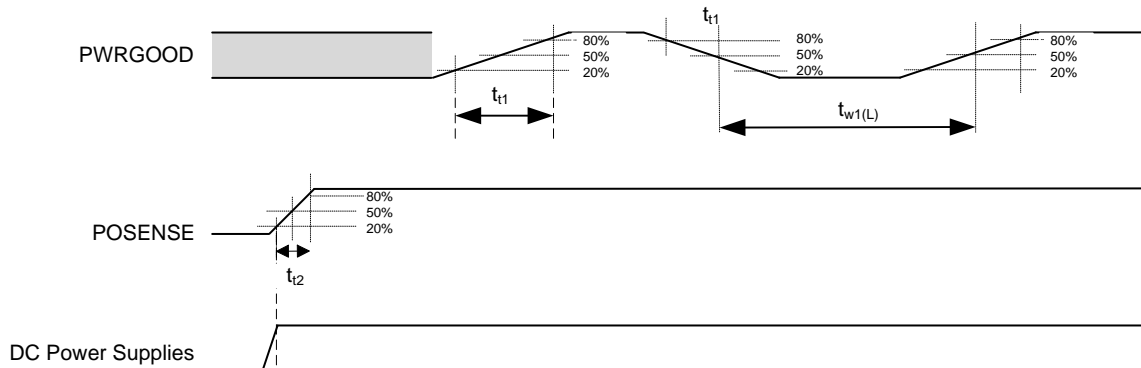


**Figure 1. System Oscillators**

## 6.7 Reset Timing Requirements

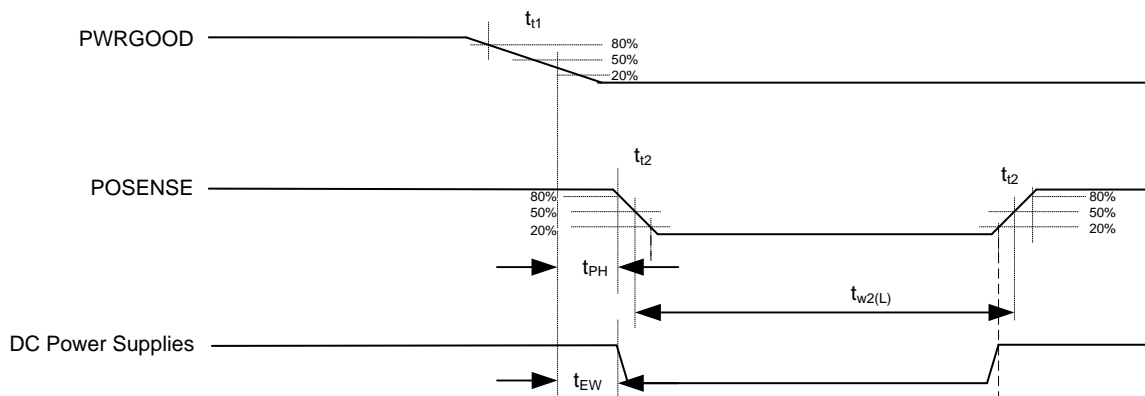
PARAMETER			MIN	MAX	UNIT
$t_{w1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)	4		$\mu\text{s}$
$t_{w1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)		1000	ms
$t_{t1}$	Transition time, PWRGOOD, $t_{t1} = t_f / t_r$	20% to 80% reference points (signal)		625	$\mu\text{s}$
$t_{w2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)	500		$\mu\text{s}$
$t_{w2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)		1000	ms
$t_{t2}$	Transition time, POSENSE, $t_{t2} = t_f / t_r$	20% to 80% reference points (signal)		25 <sup>(1)</sup>	$\mu\text{s}$
$t_{PH}$	Power hold time, POSENSE remains active after PWRGOOD is deasserted.	20% to 80% reference points (signal)	500		$\mu\text{s}$
$t_{EW}$	Early warning time, PWRGOOD goes inactive low before any power supply voltage goes below its specification.		500		$\mu\text{s}$
$t_{w1(L)} + t_{w2(L)}$	The sum of PWRGOOD and POSENSE inactive time			1050	ms

(1) As long as noise on this signal is below the hysteresis threshold.



A. PWRGOOD has no impact on operation for 60 ms after rising edge of POSENSE.

**Figure 2. Power Up**



**Figure 3. Power Down**



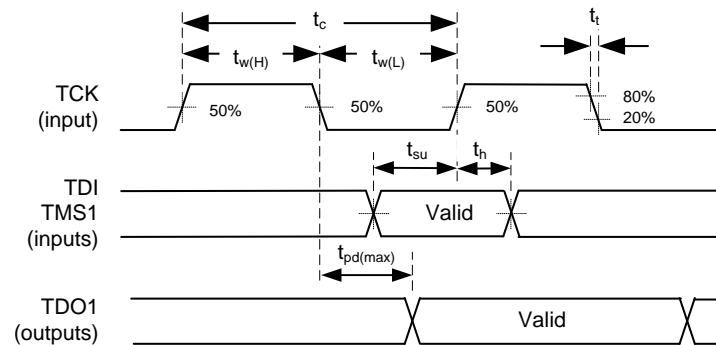
## 6.8 JTAG Interface: I/O Boundary Scan Application Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency, TCK			10	MHz
$t_c$	Cycle time, TCK		100		ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	40		ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	40		ns
$t_t$	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)		5	ns
$t_{su}$	Setup time, TDI valid before TCK↑		8		ns
$t_h$	Hold time, TDI valid after TCK↑		2		ns
$t_{su}$	Setup time, TMS1 valid before TCK↑		8		ns
$t_h$	Hold time, TMS1 valid after TCK↑		2		ns

## 6.9 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

Switching characteristics over recommended operating conditions,  $C_L$  (min timing) = 5 pF,  $C_L$  (max timing) = 85 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}$	Output propagation, clock to Q	TCK↑	TDO1	3	12	ns



**Figure 4. I/O Boundary Scan**

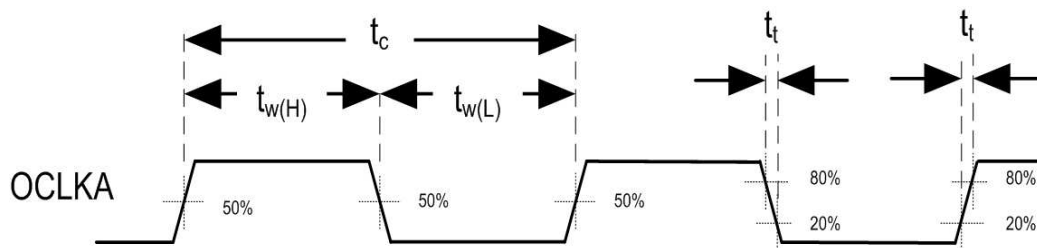
## 6.10 Programmable Output Clocks Switching Characteristics

Switching characteristics over recommended operating conditions,  $C_L$  (min timing) = 5 pF,  $C_L$  (max timing) = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency, OCLKA1 <sup>(1)</sup>	N/A	OCLKA	0.787	50.00	MHz
$t_c$	Cycle time, OCLKA	N/A	OCLKA	20.00	1270.6	ns
$t_{w(H)}$	Pulse duration, high <sup>2</sup> 50% to 50% reference points (signal)	N/A	OCLKA	$(t_c / 2) - 2$		ns
$t_{w(L)}$	Pulse duration, low <sup>2</sup> 50% to 50% reference points (signal)	N/A	OCLKA	$(t_c / 2) - 2$		ns
	Jitter	N/A	OCLKA		350	ps

(1) The frequency of OCLKA is programmable.

(2) The duty cycle of OCLKA will be within  $\pm 2$  ns of 50%.

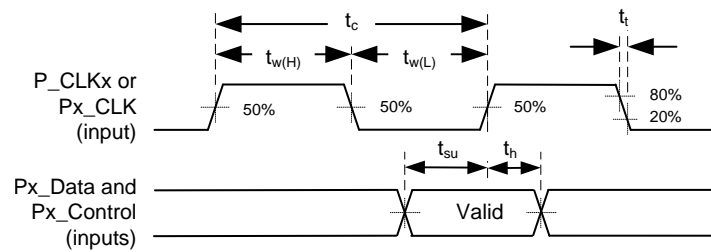


**Figure 5. Programmable Output Clocks**

## 6.11 Port 1 and 2 Input Pixel Interface Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (30-bit bus)		12	175	MHz
$f_{\text{clock}}$	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (60-bit bus) See <a href="#">Two Pixels Per Clock (60-bit Bus) Timing Requirements</a> .		12	141	MHz
$t_c$	Cycle time, P_CLK1, P_CLK2, P_CLK3		5.714	83.33	ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	2.3		ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	2.3		ns
$t_{jp}$	Clock period jitter P_CLK1, P_CLK2, P_CLK3 (that is, the deviation in period from ideal period)	Max $f_{\text{clock}}$		See <sup>(1)</sup>	ps
$t_t$	Transition time, $t_t = t_f / t_r$ , P_CLK1, P_CLK2, P_CLK3	20% to 80% reference points (signal)	0.6	2.0	ns
$t_t$	Transition time, $t_t = t_f / t_r$ , P1_A(9:0), P1_B(9:0), P1_C(9:0), P1_HSYNC, P1_VSYNC, P1_DATEN	20% to 80% reference points (signal)	0.6	3.0	ns
$t_t$	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)	0.6	3.0	ns
$t_{su}$	Setup time, P1_A(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P1_A(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P1_B(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P1_B(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P1_C(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P1_C(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P1_VSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P1_VSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P1_HSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P1_HSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P2_A(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P2_A(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P2_B(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P2_B(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P2_C(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P2_C(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P2_VSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P2_VSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P2_HSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P2_HSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P_DATEN1, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P_DATEN1, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{su}$	Setup time, P_DATEN2, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_h$	Hold time, P_DATEN2, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
$t_{w(A)}$	VSYNC active pulse duration		1		Video line
$t_{w(A)}$	HSYNC active pulse duration		16		Pixel clocks

(1) For frequencies ( $f_{\text{clock}}$ ) less than 175 MHz, use the following formula to obtain the jitter: Max clock jitter =  $\pm [(1 / f_{\text{clock}}) - 5414 \text{ ps}]$ .


**Figure 6. Input Port 1 and 2 Interface**

## 6.12 Two Pixels Per Clock (60-bit Bus) Timing Requirements

When operating in two pixels per clock mode, the pixel clock must be maintained below 141MHz. A typical video source requiring two pixels per clock is shown in the following table and must have reduced blanking to stay below the maximum pixel clock.

Source	Rate (Hz)	Total Pixels Per Line <sup>(1)</sup>	Total Lines Per Frame <sup>(1)</sup>	Pixel Clock Achieved (MHz)
1080p	120	2060	1120	138.4

(1) Values chosen for front and back porches must meet the timing requirements in [Source Input Blanking Requirements](#)

## 6.13 SSP Switching Characteristics

Switching characteristics over recommended operating conditions,  $C_L$  (min timing) = 5 pF,  $C_L$  (max timing) = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency, SSPx_CLK	N/A	SSPx_CLK	73.00	25000	kHz
$t_c$	Cycle time, SSPx_CLK	N/A	SSPx_CLK	0.040	13.6	$\mu\text{s}$
$t_w(\text{H})$	Pulse duration, high 50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
$t_w(\text{L})$	Pulse duration, low 50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
SSP Master						
$t_{\text{pd}}$	Output propagation, clock to Q, SSPx_DO	SSPx_CLK $\downarrow$ <sup>(1)(2)</sup>	SSPx_DO <sup>(1)(2)</sup>	–5	5	ns
		SSPx_CLK $\uparrow$ <sup>(1)(3)</sup>	SSPx_DO <sup>(1)(3)</sup>	–5	5	ns
SSP Slave						
$t_{\text{pd}}$	Output propagation, clock to Q, SSPx_DO	SSPx_CLK $\downarrow$ <sup>(1)(2)</sup>	SSPx_DO <sup>(1)(2)</sup>	0	34	ns
		SSPx_CLK $\uparrow$ <sup>(1)(3)</sup>	SSPx_DO <sup>(1)(3)</sup>	0	34	ns

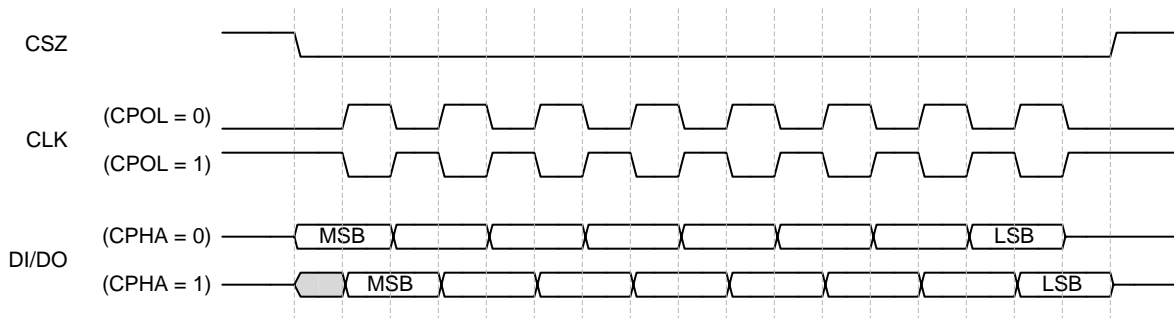
(1) The SSP is configured into four different modes of operation by the controller firmware. These modes are shown in [Table 16](#), [Figure 8](#) and [Figure 9](#).

(2) Modes 0 and 3

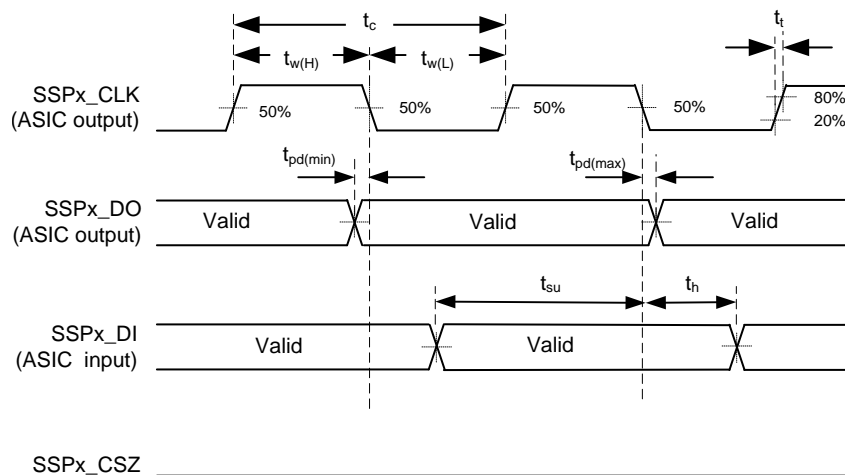
(3) Modes 1 and 2

**Table 16. SSP Clock Operational Modes**

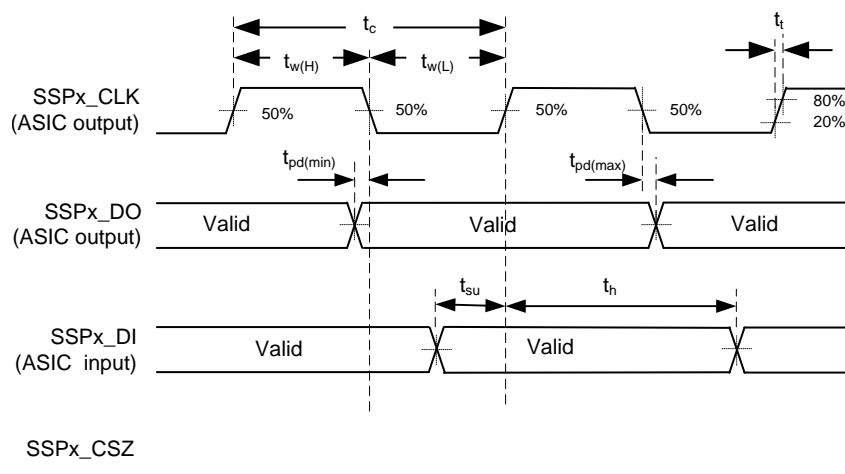
SPI Clocking Mode	SPI Clock Polarity (CPOL)	SPI Clock Phase (CPHA)
0	0	0
1	0	1
2	1	0
3	1	1



**Figure 7. SSP Clock Mode Timing Diagram**



**Figure 8. Synchronous Serial Port Interface – Master (Modes 0/3)**



**Figure 9. Synchronous Serial Port Interface – Slave (Modes 0/3)**

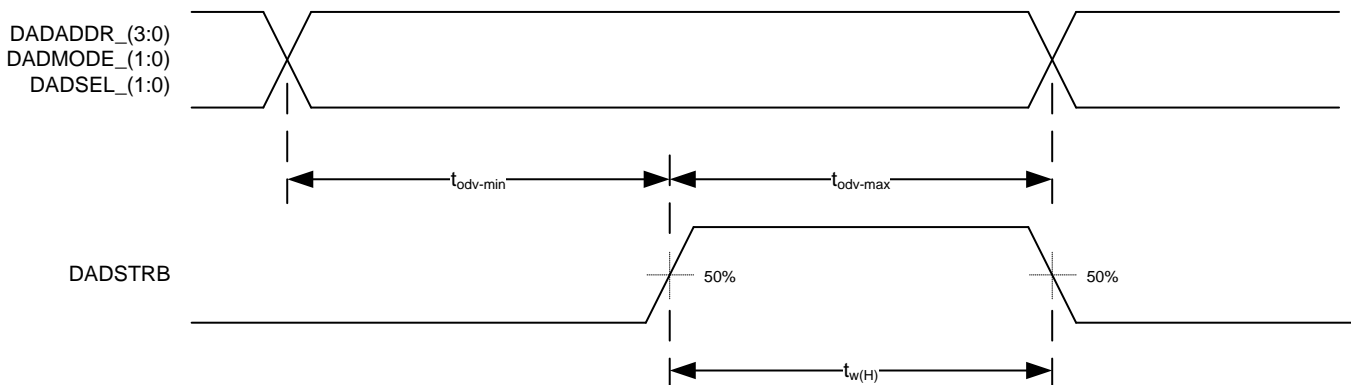
## 6.14 DMD Interface Switching Characteristics<sup>(1)</sup>

Switching characteristics over recommended operating conditions,  $C_L$  (min timing) = 5 pF,  $C_L$  (max timing) = 50 pF (unless otherwise noted)

PARAMETER	FROM	TO	MIN	MAX	UNIT
<b>DMD Timing Mode 0<sup>(2)</sup></b>					
$t_{w(H)}$	DMD strobe high pulse duration	N/A	DADSTRB	29	ns
$t_{w(L)}$	DMD strobe low pulse duration	N/A	DADSTRB	29	ns
$T_{odv-min}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑	-27	ns
$T_{odv-max}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑	27	ns
<b>DMD Timing Mode 1<sup>(2)</sup></b>					
$t_{w(H)}$	DMD strobe pulse duration	N/A	DADSTRB	14	ns
$t_{w(L)}$	DMD strobe low pulse duration	N/A	DADSTRB	14	ns
$T_{odv-min}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑	-12	ns
$T_{odv-max}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑	12	ns

(1) DMD control signals are captured on the rising edge of DADSTRB within the DMD.

(2) The DMD timing mode is controlled by the controller firmware.



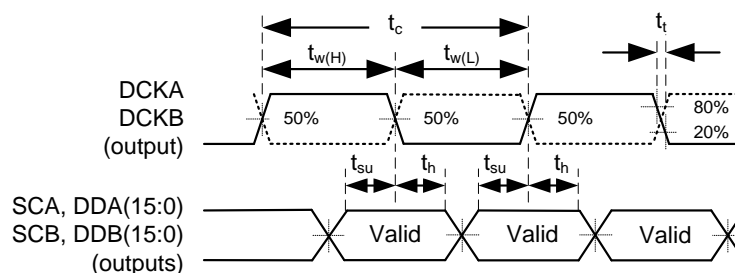
**Figure 10. DMD Interface Timing**

## 6.15 DMD LVDS Interface Switching Characteristics<sup>(1)(2)(3)(4)(5)(6)</sup>

Switching characteristics over recommended operating conditions

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency, DCK_A	DCK_A	100	400	MHz
$t_c$	Cycle time, DCK_A1	DCK_A	2475.3		ps
$t_{w(H)}$	Pulse duration, high 5 (50% to 50% reference points)	DCK_A	1093		ps
$t_{w(L)}$	Pulse duration, low 5 (50% to 50% reference points)	DCK_A	1093		ps
$t_t$	Transition time, $t_t = t_f / t_r$ (20% to 80% reference points)	DCK_A	100	400	ps
$t_{\text{osu}}$	Output setup time at max clock rate3	DCK_A $\uparrow\downarrow$	SCA, DDA(15:0)	438	ps
$t_{\text{oh}}$	Output hold time at max clock rate3	DCK_A $\uparrow\downarrow$	SCA, DDA(15:0)	438	ps
$f_{\text{clock}}$	Clock frequency, DCK_B	DCK_B	100	400	MHz
$t_c$	Cycle time, DCK_B1	DCK_B	2475.3		ps
$t_{w(H)}$	Pulse duration, high 5 (50% to 50% reference points)	DCK_B	1093		ps
$t_{w(L)}$	Pulse duration, low 5 (50% to 50% reference points)	DCK_B	1093		ps
$t_t$	Transition time, $t_t = t_f / t_r$ (20% to 80% reference points)	DCK_B	100	400	ps
$t_{\text{osu}}$	Output setup time at max clock rate3	DCK_B $\uparrow\downarrow$	SCB, DDB(15:0)	438	ps
$t_{\text{oh}}$	Output hold time at max clock rate3	DCK_B $\uparrow\downarrow$	SCB, DDB(15:0)	438	ps
$t_{\text{sk}}$	Output skew, channel A to channel B	DCK_A $\uparrow$	DCK_B $\uparrow$	250	ps

- (1) The minimum cycle time ( $t_c$ ) for DCK\_A and DCK\_B includes 1.0% spread spectrum modulation.
- (2) The DMD LVDS interface uses a double data rate (DDR) clock, thus both rising and falling edges of DCK\_A and DCK\_B are used to clock data into the DMD. As a result, the minimum  $t_{w(H)}$  and  $t_{w(L)}$  parameters determine the worse-case DDR clock cycle time.
- (3) Output setup and hold times for DMD clock frequencies below the maximum can be calculated as follows:  
 $t_{\text{osu}}(f_{\text{clock}}) = t_{\text{osu}}(f_{\text{max}}) + 250000 \times (1 / f_{\text{clock}} - 1 / 400)$  and  $t_{\text{oh}}(f_{\text{clock}}) = t_{\text{oh}}(f_{\text{max}}) + 250000 \times (1 / f_{\text{clock}} - 1 / 400)$  where  $f_{\text{clock}}$  is in MHz.
- (4) The DLPC900 is a Full-Bus DMD signaling interface. Figure 16 shows the controller connections for this configuration.
- (5) The pulse duration minimum for any clock rate can be calculated using the following formulas.
  - (a) Pulse duration minimum when using spread spectrum
    - (a) Duty cycle % =  $49.06 - [0.01335 \times \text{clock frequency (MHz)}]$
    - (b) Minimum pulse duration =  $1 / \text{clock frequency} \times \text{DC\%}$
    - (a) Example: At 400 MHz:  $\text{DC\%} = 49.06 - [0.01335 \times 400] = 43.72\%$
    - (b)  $\text{MPW} = 1 / 400 \text{ MHz} \times 0.4372 = 1093.0 \text{ ps}$
  - (b) Pulse duration minimum when not using spread spectrum
    - (a) Duty cycle % =  $49.00 - [0.01055 \times \text{clock frequency (MHz)}]$
    - (b) Minimum pulse duration =  $1 / \text{clock frequency} \times \text{DC\%}$
    - (a) Example: At 400 MHz:  $\text{DC\%} = 49.00 - [0.01055 \times 400] = 44.78\%$
    - (b)  $\text{MPW} = 1 / 400 \text{ MHz} \times 0.448 = 1119.5 \text{ ps}$
- (6) A duty cycle specification is not provided because the key limiting factor to clock frequency is the minimum pulse duration (that is, if the other half of the clock period is larger than the minimum, it is not limiting the clock frequency).

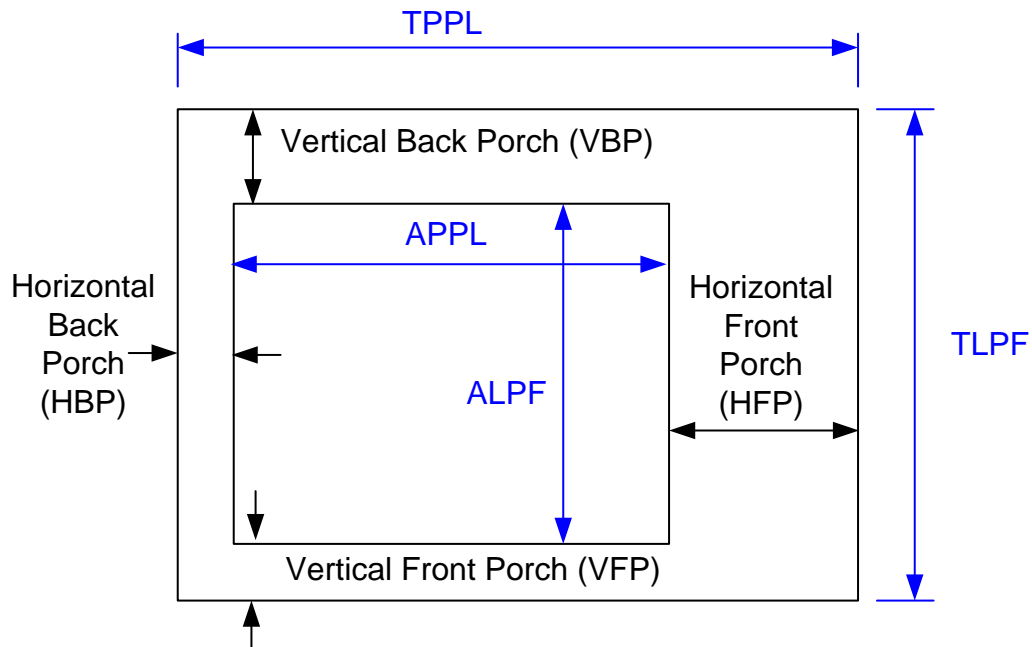


**Figure 11. DMD LVDS Interface**

## 6.16 Source Input Blanking Requirements

PORT	Parameter <sup>(1)</sup>	MINIMUM BLANKING
Port 1 Vertical Blanking	VBP	370 $\mu$ s
	VFP	1 Line
	Total vertical blanking	370 $\mu$ s + 2 lines
Port 2 Vertical Blanking	VBP	370 $\mu$ s
	VFP	1 line
	Total vertical blanking	370 $\mu$ s + 2 lines
Port 1 and 2 Horizontal Blanking	HBP	10 pixels
	HFP	0 pixels
	Total horizontal blanking	80 pixels

(1) Refer to the video timing parameter definitions listed in Video Timing Parameter Definitions.



**Figure 12. Video Timing Parameters**



## 7 Detailed Description

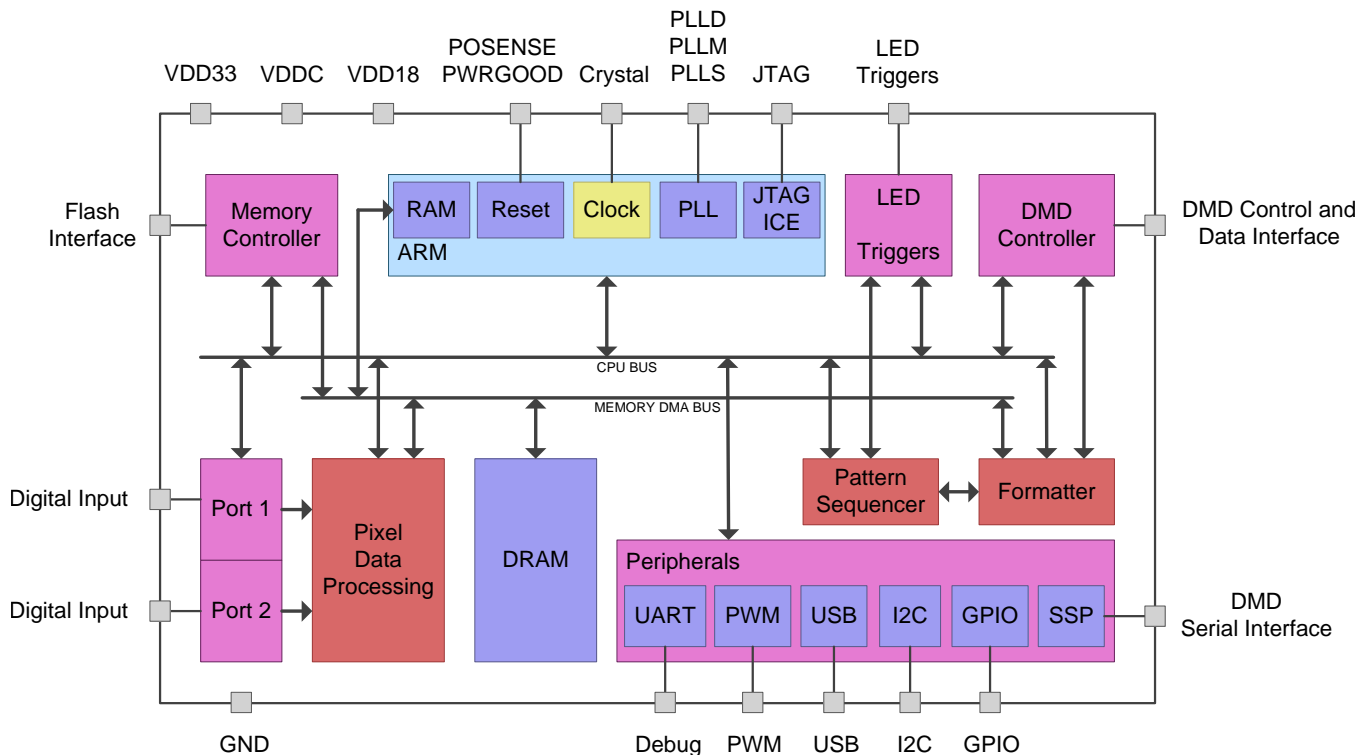
### 7.1 Overview

The DLPC900 controller processes the digital input image and converts the data into the digital format needed by the DLP9000 or the DLP6500. The DLP9000 and the DLP6500 reflect light by using binary pulse-width-modulation (PWM) for each micromirror. For further details, refer to the DLP9000 or the DLP6500 data sheets.

The DLPC900 combined with a DLP6500 supports a wide variety of resolutions from SVGA to 1080p. When accurate pattern display is needed, a native 1080p resolution source is used for a one-to-one association with the corresponding micromirror on the DLP6500.

The DLPC900 combined with a DLP9000 supports only native WQXGA resolution for a one-to-one association with the corresponding micromirror on the DLP9000. Both combinations are well-suited for structured light, additive manufacturing, or digital exposure applications.

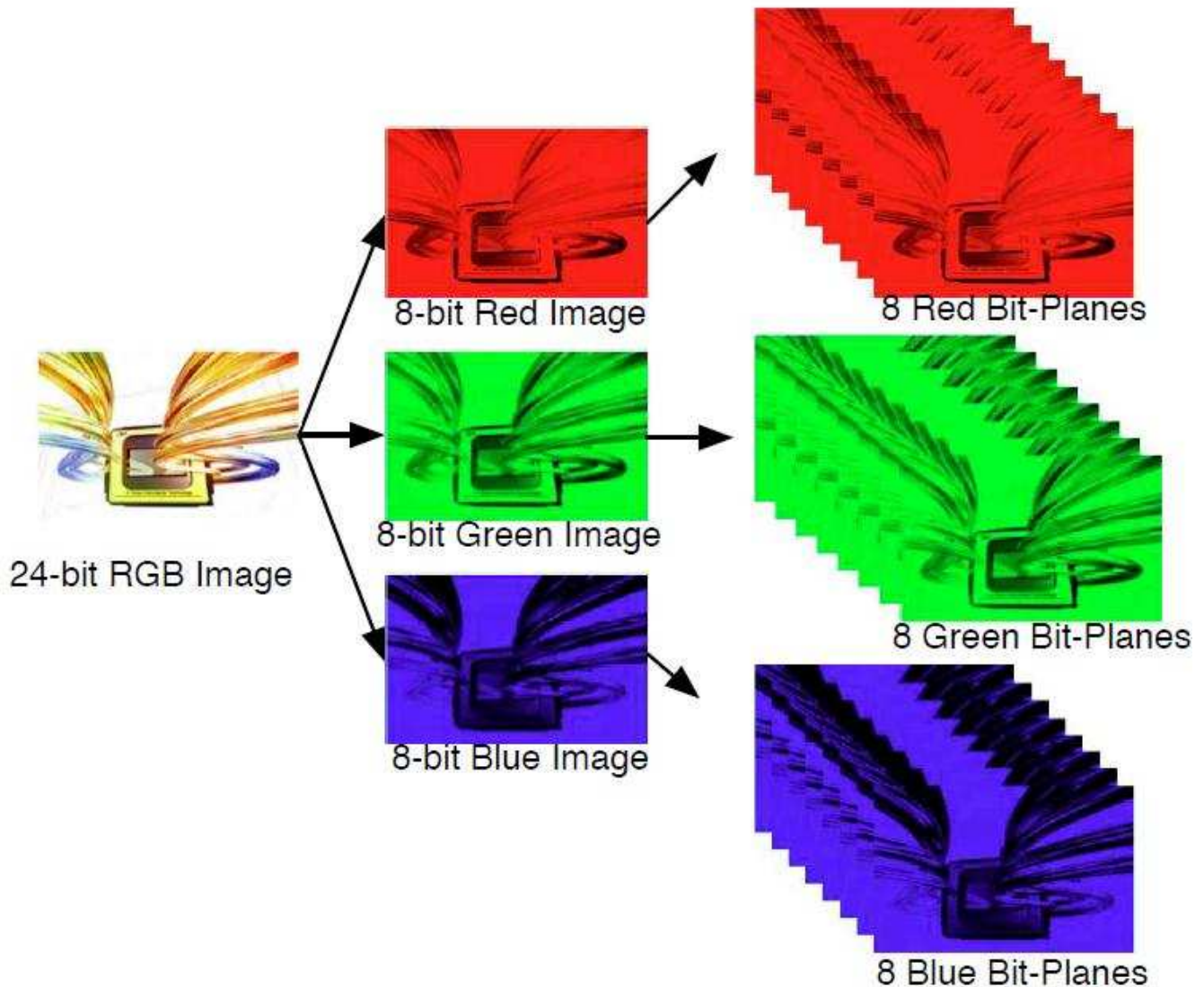
### 7.2 Functional Block Diagram



**Figure 13. Functional Block Diagram**

The DLPC900 controller takes as input 16-, 20-, 24-, or 30-bit RGB data at up to 120-Hz frame rate. For example, a 120Hz frame is composed of three colors (red, green, and blue) with each color equally divided in the 120-Hz frame rate. Thus, each color has a 2.78-ms time slot allocated. Because each color has an 8-, 9-, or 10-bit depth, each color time slot is further divided into bit-planes. A bit-plane is the 2-dimensional arrangement of one-bit extracted from all the pixels in the full color 2D image to implement dynamic depth, see [Figure 14](#).

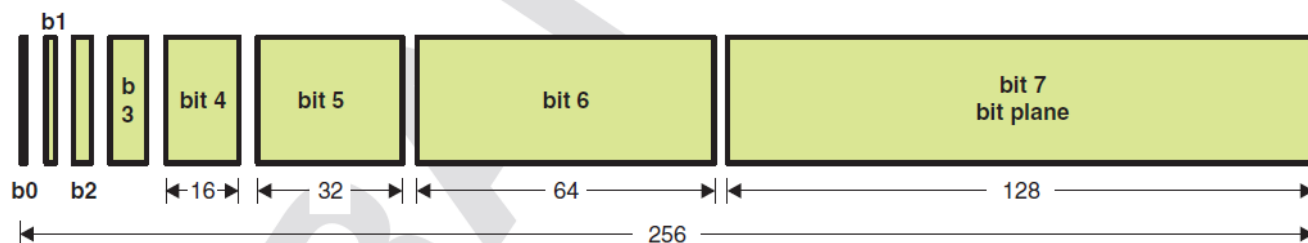
## Functional Block Diagram (continued)



**Figure 14. Bit Slices**

The length of each bit-plane in the time slot is weighted by the corresponding power of two of its binary representation. This provides a binary pulse-width modulation of the image. For example, a 24-bit RGB input has three colors with 8-bit depth each. Each color time slot is divided into eight bit-planes, with the sum of the weight of all bit planes in the time slot equal to 256. See [Figure 15](#) for an illustration of this partition of the bits in a frame.

## Functional Block Diagram (continued)



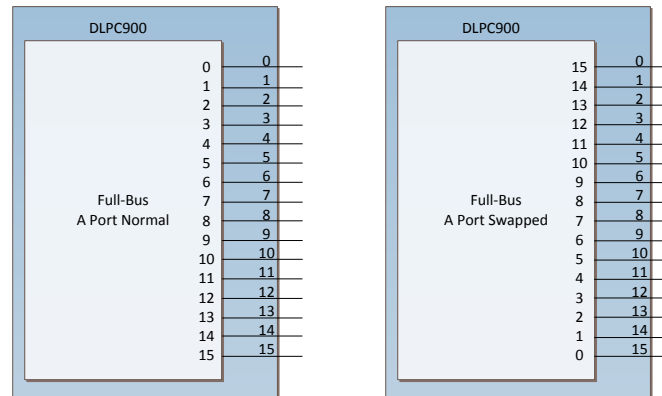
**Figure 15. Bit Partition in a Frame for an 8-Bit Color**

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane. With binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame image inputted to the DLPC900 controller, the DLPC900 controller creates 24 bit-planes, stores them in internal embedded DRAM, and sends them to the DMD, one bitplane at a time. The bit weight controls the amount of time the mirror is on. To improve image quality in video frames, these bit-planes, time slots, and color frames are shuffled and interleaved within the pixel processing functions of the DLPC900 controller.

## 7.3 Feature Description

### 7.3.1 DMD Configurations

Figure 16 shows the controller connections for full-bus normal or swapped. Refer to the DLPC900 Programmers Guide for details on how to select the bus swap settings to match the board layout connections.



**Figure 16. Controller to DMD Full-Bus Connections**

### 7.3.2 Video Timing Input Blanking Specification

The DLPC900 controller requires a minimum horizontal and vertical blanking for both Port 1 and Port 2 as shown in [Source Input Blanking Requirements](#). These parameters indicate the time allocated to retrace the signal at the end of each line and field of a display. Reference the video timing parameter definitions listed in Video Timing Parameter Definitions.

### 7.3.3 Board-Level Test Support

The In-Circuit Tri-State Enable signal (ICTSEN) is a board-level test control signal. By driving ICTSEN to a logic high state, all controller outputs (except TDO1 and TDO2) will be configured as tri-state outputs.

The DLPC900 also provides JTAG boundary scan support on all I/O except non-digital I/O and a few special signals. [Table 17](#) lists these exceptions.

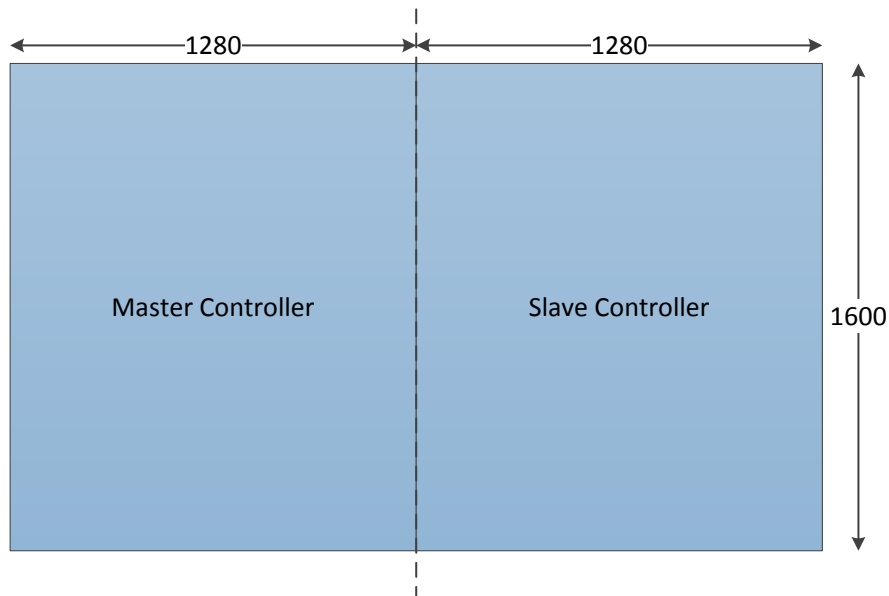
**Table 17. DLPC900 – Signals Not Covered by JTAG<sup>(1)</sup>**

Signal Name	Package Ball
HW_TEST_EN	M25
MOSC	M26
MOSCN	N26
USB_DAT_N	C5
USB_DAT_P	D6
TCK	N24
TDI	N25
TRSTZ	M23
TDO1	N23
TDO2	N22
TMS1	P25
TMS2	P26

(1) There is no JTAG connection to power or no-connect pins.

### 7.3.4 Two Controller Considerations

When two DLPC900 controllers drive a single high-resolution DLP9000 DMD, each controller is used to drive half of the DMD, as shown in [Figure 17](#). Each controller must operate in two pixels per clock, and the pixel clock must be maintained below the maximum two pixel per clock frequency. Only WQXGA resolution is supported when two DLPC900 controllers are matched with a DLP9000 DMD.



**Figure 17. Two Controllers Connected to DLP9000 DMD**

## 7.4 Device Functional Modes

### 7.4.1 Structured Light Application

For structured light applications, the DLPC900 can be commanded to enter high speed sequential pattern modes where a specific set of patterns are selected with a maximum of 24 bits per pixel. The bit-depth of the patterns are then allocated into the corresponding time slots. Furthermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed.

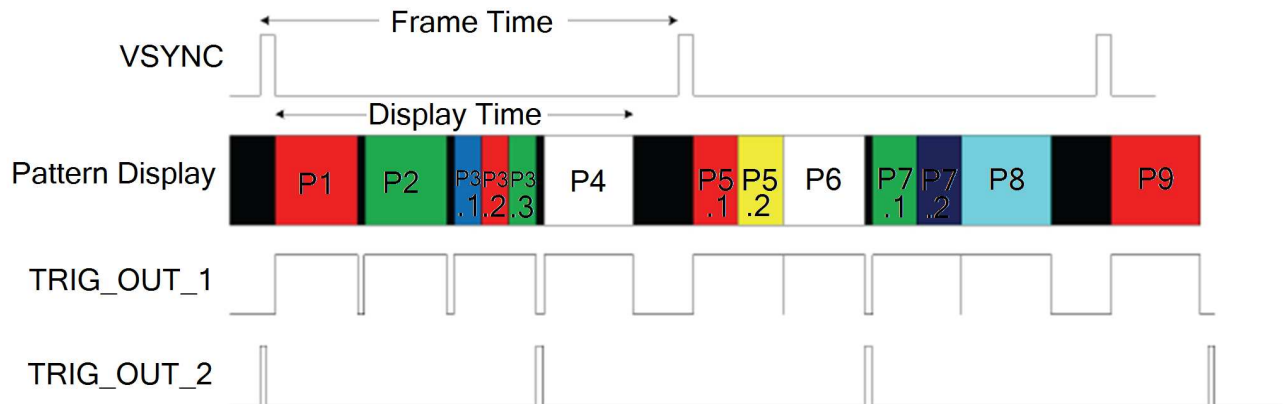
This pattern mode provides the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object. The DLPC900 controller is capable of pre-loading up to 400 1-bit binary patterns into internal memory from the external flash memory. These pre-loaded binary patterns are then steamed to the DMD at high speed.

To synchronize a camera to the displayed patterns, the DLPC900 controller supports two pattern modes: Video pattern and Pre-stored pattern modes. In video pattern mode, the vertical sync is used as trigger input. In pre-stored pattern mode, an internal user configurable trigger or a TRIG\_IN\_1 pulse indicates to the DLPC900 controller to advance to the next pattern, while TRIG\_IN\_2 starts and stops the pattern sequence. In both pattern modes, TRIG\_OUT\_1 frames the exposure time of the pattern, while TRIG\_OUT\_2 indicates the start of the pattern sequence.

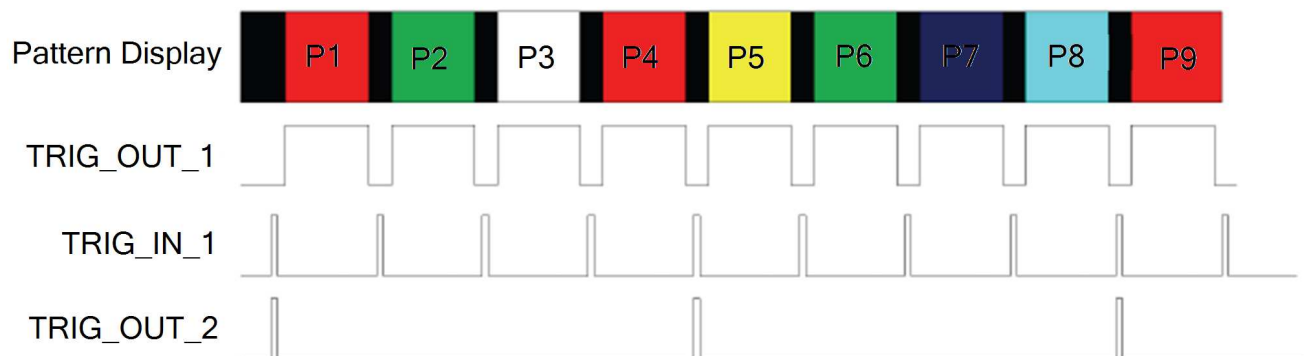
[Figure 18](#) shows an example of a video pattern mode. The VSYNC starts the pattern sequence display. The pattern sequence consists of a series of three consecutive patterns. The first pattern sequence consists of P1, P2, and P3. Because P3 is an RGB pattern, it is shown with its time sequential representation of P3.1, P3.2, and P3.3. The second pattern sequence consists of three patterns: P4, P5, and P6. The third sequence consists of P7, P8, and P9. TRIG\_OUT\_1 frames each pattern exposed, while TRIG\_OUT\_2 indicates the start of each of the three pattern sequences.

## Device Functional Modes (continued)

Figure 19 shows an example of a pre-stored pattern mode. Pattern sequences of four are displayed. TRIG\_OUT\_1 frames each pattern exposed, while TRIG\_OUT\_2 indicates the start of each four-pattern sequence. TRIG\_IN\_1 pulses advance the pattern. Another example of a pre-stored pattern mode is shown in Figure 20, where pattern sequences of three are displayed. TRIG\_OUT\_1 frames each pattern displayed, while TRIG\_OUT\_2 indicates the start of each three-pattern sequence. TRIG\_IN\_2 serves as a start and stop signal. When high, the pattern sequence starts or continues. Note that in the middle of displaying the P4 pattern, TRIG\_IN\_2 is low, so the sequence stops displaying P4. When TRIG\_IN\_2 is raised, the pattern sequence continues where it stopped by re-displaying P4. Table 18 shows the allowed pattern combinations in relation to the bit depth of the pattern.

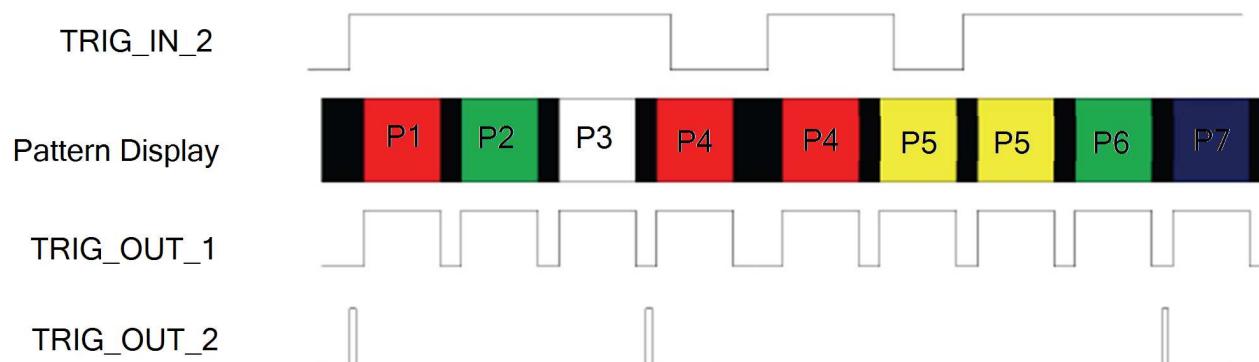


**Figure 18. Video Pattern Mode Timing Diagram**



**Figure 19. Pre-Stored Pattern Mode Timing Diagram**

## Device Functional Modes (continued)



**Figure 20. Pre-Stored Pattern Mode Timing Diagram for 3-Patterns**

**Table 18. Allowed Pattern Combinations**

BIT DEPTH	EXTERNAL RGB PATTERN RATE (Hz)	PRE-LOADED PATTERN RATE (Hz) WITH INTERNAL TRIGGERING	PRE-LOADED PATTERN RATE (Hz) WITH EXTERNAL TRIGGERING <sup>(1)</sup>	MAXIMUM NUMBER OF PATTERNS (PRE-LOADED) <sup>(2)</sup>
1	2880	9523	8333	400
2	1440	3289	3125	200
3	960	2638	2380	133
4	720	1364	1190	100
5	480	823	813	80
6	480	672	664	66
7	360	500	496	57
8	247	247	246	50

(1) The reduction in pattern rates are due to interrupt processing and sequence setup time from when the external interrupt occurs.

(2) Numbers reflect uncompressed patterns.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The DLPC900 controller is required to be coupled with the DLP6500 or the DLP9000 DMDs to provide a reliable display solution for video display and structure light applications. The DLPC900 converts the digital input data into the digital format needed by the DLP6500 or the DLP9000 DMDs. The DMDs consist of an array of micromirrors which reflect incoming light to one of two directions by using binary pulse-width-modulation (PWM) for each micromirror, where the primary direction being into a projection or collection optics. Applications of interest include 3D machine vision, 3D printing, direct imaging lithography, and intelligent lighting.

### 8.2 Typical Application

#### 8.2.1 Typical Two Controller Chipset

A typical embedded system application using the DLPC900 controller and DLP9000 is shown in [Figure 21](#). This configuration requires two DLPC900 controllers to drive a DLP9000 DMD and supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. In this configuration, the 24-bit parallel RGB input data is split between the master and the slave controller as described in [Two Controller Considerations](#) using an FPGA or some other mechanism.

This system supports both still and motion video sources with the input resolution native to the DLP9000. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC900 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

This configuration also supports high speed sequential pattern mode. The patterns are pre-stored in external flash and have a maximum of 24 bits per pixel. The patterns are pre-loaded into internal embedded DRAM and then streamed to the DLP9000 using the pattern modes mentioned in the [Structured Light Application](#).



## Typical Application (continued)

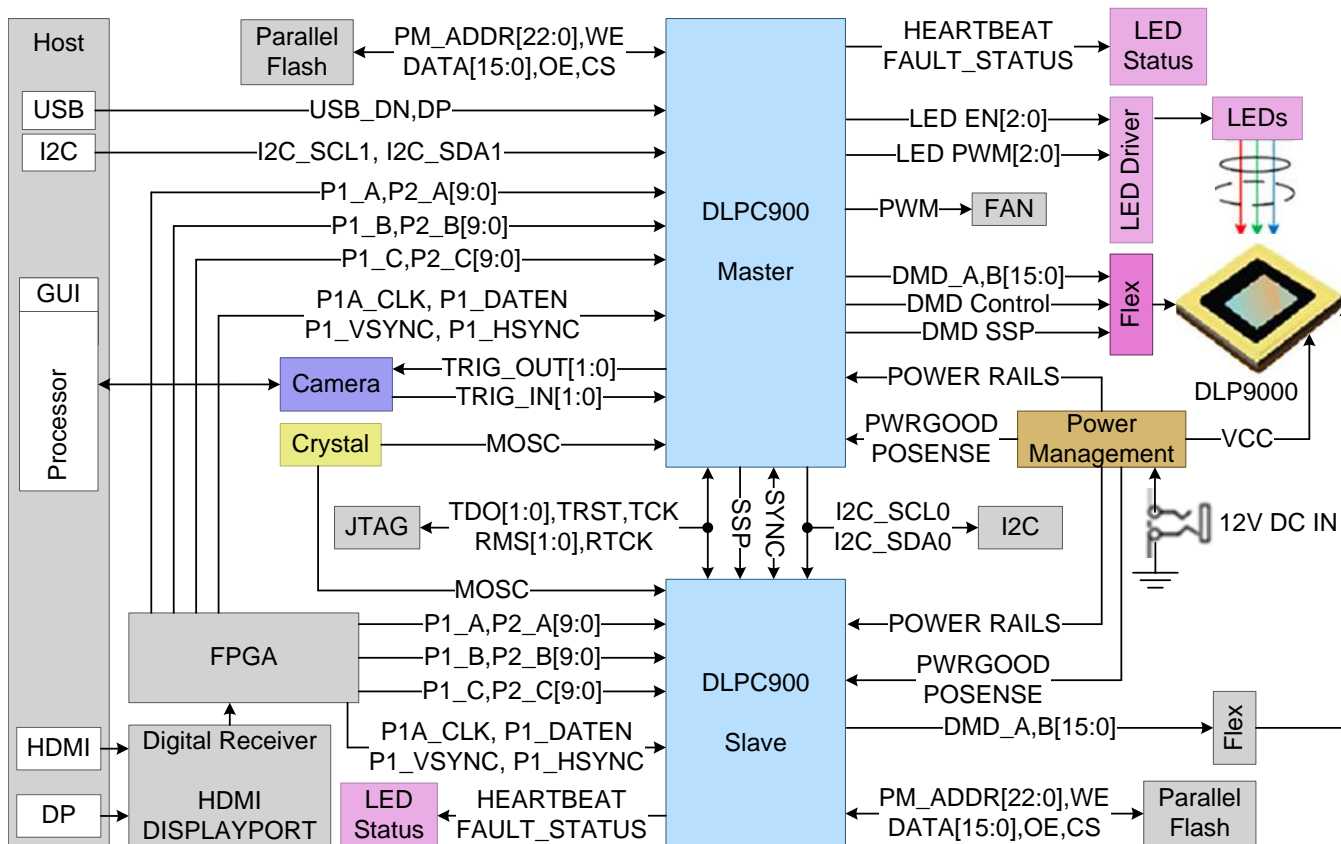


Figure 21. Typical Application Schematic for DLP9000

### 8.2.2 Typical Single Controller Chipset

A typical embedded system application using the DLPC900 controller and DLP6500 is shown in [Figure 22](#). This configuration uses one DLPC900 controller to operate with a DLP6500 and supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor.

This system supports both still and motion video sources. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC900 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

This configuration also supports high speed sequential pattern mode. The patterns are pre-stored in external flash and have a maximum of 24 bits per pixel. The patterns are pre-loaded into internal embedded DRAM and then streamed to the DLP6500 using the pattern modes mentioned in the [Structured Light Application](#).

## Typical Application (continued)

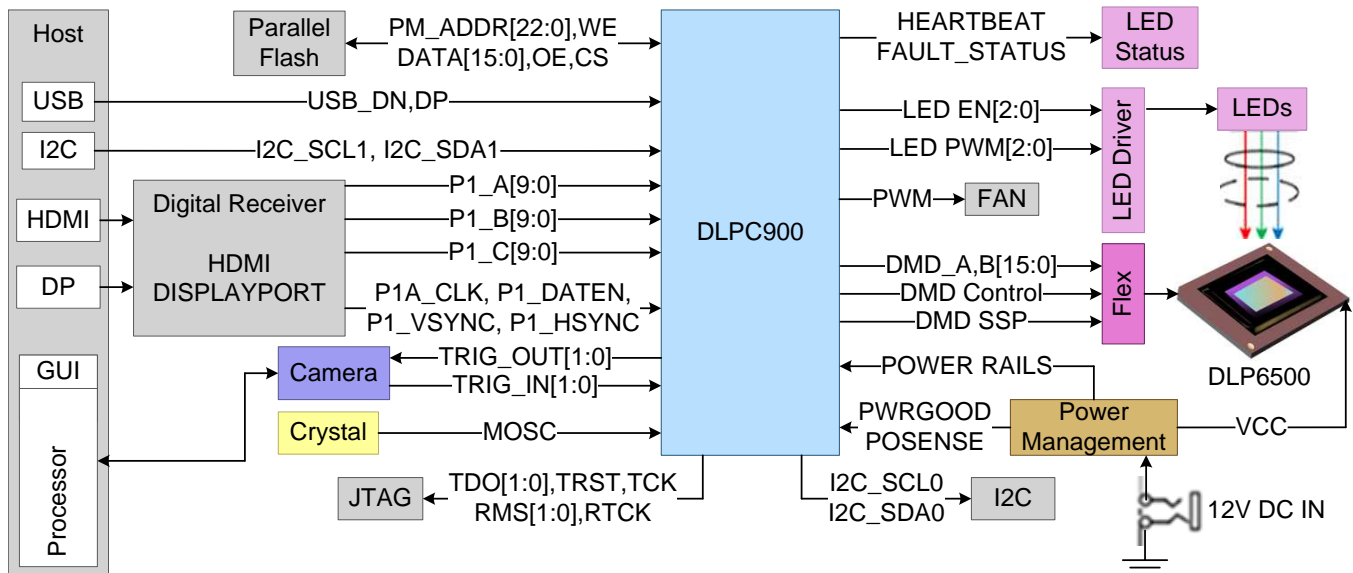


Figure 22. Typical Application Schematic for DLP6500

### 8.2.3 Design Requirements

All applications require both the controller and DMD components for reliable operation. The system uses an external parallel flash memory device loaded with the DLPC900 configuration and support firmware. The external boot flash must contain a minimum of 2 sectors, where the first sector starts at address 0x00000000 which is the power-up reset start address. The first 64kBytes is reserved for the bootloader image and must be in its own sector and can be made up of several smaller contiguous sectors that add up to 64kbytes as shown in Figure 23. The remaining sectors contains the rest of the firmware. The default wait-states is set for a flash device of 120ns access time. For a faster flash access time, refer to the [Program Memory Flash Interface](#) on how to program new wait-state values.

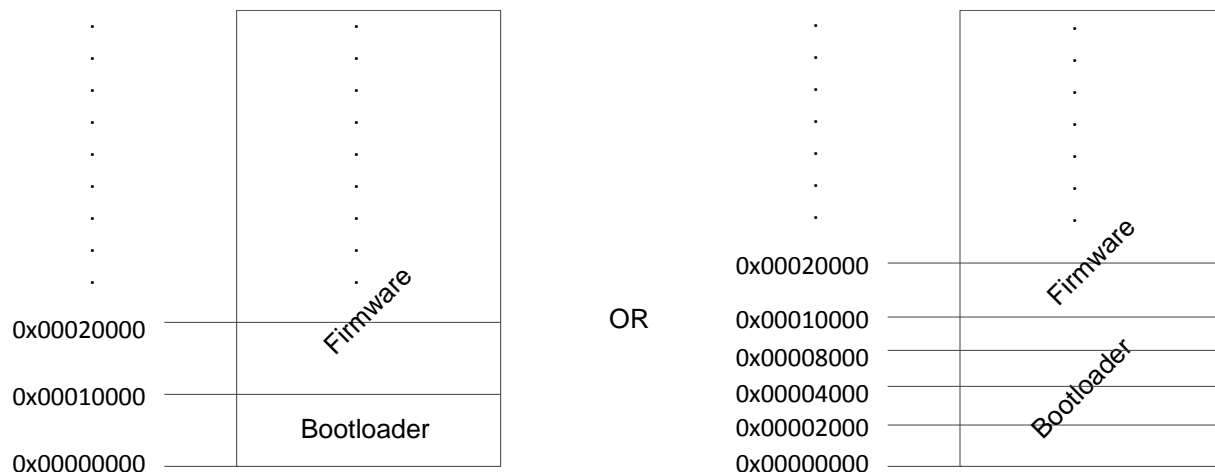


Figure 23. Boot Flash Memory Layout

The chipset has the following interfaces and support circuitry:

- DLPC900 System Interfaces
  - Control Interfaces
  - Trigger Interface

## Typical Application (continued)

- Input Data Interfaces
- Illumination Interface
- DLPC900 Support Circuitry and Interfaces
  - Reference Clock
  - PLL
  - Program Memory Flash Interface
- DMD Interface
  - DLPC900 to DLP6500/DLP9000 Digital Data
  - DLPC900 to DLP6500/DLP9000 Control and Clock Interface
  - DLPC900 to DLP6500/DLP9000 Serial Communication Interface

## 8.3 Detailed Design Procedure

### 8.3.1 DLPC900 System Interfaces

The DLPC900 chipset supports a 30-bit parallel RGB interface for image data transfers from another device and a 30-bit interface for video data transfers. The system input requires proper generation of the PWRGOOD and POSENSE inputs to ensure reliable operation. There are two primary output interfaces: illumination driver control interface and sync outputs.

#### 8.3.1.1 Control Interface

The DLPC900 chipset supports I<sup>2</sup>C or USB commands through the control interface. The control interface allows another master processor to send commands to the DLPC900 controller to query system status or perform real-time operations, such as, LED driver current settings. The DLPC900 allows the user to set a different I<sup>2</sup>C slave address for the host port. Refer to the DLPC900 Programmers Guide to set a different I<sup>2</sup>C master and slave addresses.

**Table 19. Active Signals – I<sup>2</sup>C Interfaces**

SIGNAL NAME	DESCRIPTION
I2C2_SCL	I2C clock. Bidirectional open-drain signal. I <sup>2</sup> C master clock to external devices.
I2C2_SDA	I2C data. Bidirectional open-drain signal. I <sup>2</sup> C master to transfer data to external devices.
I2C1_SCL	I2C clock. Bidirectional open-drain signal. I <sup>2</sup> C master clock to external devices.
I2C1_SDA	I2C data. Bidirectional open-drain signal. I <sup>2</sup> C master to transfer data to external devices.
I2C0_SCL <sup>(1)</sup>	I2C clock. Bidirectional open-drain signal. I <sup>2</sup> C slave clock input from the external processor.
I2C0_SDA <sup>(1)</sup>	I2C data. Bidirectional open-drain signal. I <sup>2</sup> C slave to accept commands or transfer data to and from the external processor.

(1) This interface is the host port.

#### 8.3.1.2 Input Data Interfaces

The data interface has a Parallel RGB input port and has a nominal I/O voltage of 3.3 V. Maximum and minimum input timing specifications for both components are provided in the Interface Timing Requirements. Each parallel RGB port can support up to 30 bits in video mode. In pattern mode, the upper 8-bits of each color are used to convert the 30-bit input into a 24-bit RGB input.

**Table 20. Active Signals – Data Interface**

SIGNAL NAME	DESCRIPTION
RGB Parallel Interface Port 1	
P1_(A, B, C)_[0:9] <sup>(1)</sup>	30-bit data inputs 10 bits for each of the red, green, and blue channels. If interfacing to a system with less than 10-bits per color, connect the bus of the red, green, and blue channels to the upper bits of the DLPC900 10-bit bus.
P_CLK1	Pixel clock; all input signals on data interface are synchronized with this clock.

(1) The A, B, and C input data channels of Port 1 and 2 can be internally swapped for optimum board layout. Refer to the DLPC900 Programmers Guide for details on how to configuring the port settings to match the board layout connections.

**Table 20. Active Signals – Data Interface (continued)**

SIGNAL NAME	DESCRIPTION
P1_VSYNC	Vertical sync
P1_HSYNC	Horizontal sync
P_DATAEN1	Input data valid
RGB Parallel Interface Port 2	
P2_(A, B, C)_[0:9] <sup>(1)</sup>	30-bit data inputs 10 bits for each of the red, green, and blue channels. If interfacing to a system with less than 10-bits per color, connect the bus of the red, green, and blue channels to the upper bits of the DLPC900 10-bit bus.
P_CLK2	Pixel clock; all input signals on data interface are synchronized with this clock.
P2_VSYNC	Vertical sync
P2_HSYNC	Horizontal sync
P_DATAEN2	Input data valid
Optional Pixel Clock 3	
P_CLK3	Pixel clock; all input signals on data interface are synchronized with this clock.

### 8.3.1.3 DLPC900 System Output Interfaces

#### 8.3.1.3.1 Illumination Interface

An illumination interface is provided that supports up to a three (3) channel LED driver. The illumination interface provides signals that support: LED driver enable, LED enable, LED enable select, and PWM signals to control the LED current.

**Table 21. Active Signals - Illumination Interface**

SIGNAL NAME	DESCRIPTION
HEARTBEAT	Signal toggles continuously to indicate system is running fine.
FAULT_STATUS	Signal toggles or held high indicating system faults
RED_LED_EN	Red LED enable
GRN_LED_EN	Green LED enable
BLU_LED_EN	Blue LED enable
RED_LED_PWM	Red LED PWM signal used to control the LED current
GRN_LED_PWM	Green LED PWM signal used to control the LED current
BLU_LED_PWM	Blue LED PWM signal used to control the LED current

#### 8.3.1.3.2 Trigger and Sync Interface

The DLPC900 outputs a trigger signal for synchronizing displayed patterns with a camera, sensor, or other peripherals. The sync output supporting signals are: horizontal sync, vertical sync, two input triggers, and two output triggers. Depending on the application, these signals control how the pattern is displayed.

**Table 22. Active Signals - Trigger and Sync Interface**

SIGNAL NAME	DESCRIPTION
P1_HSYNC	Horizontal Sync
P1_VSYNC	Vertical Sync
TRIG_IN_1	Depending on the mode, advances the pattern display.
TRIG_IN_2	Depending on the mode, starts or stops the pattern display.
TRIG_OUT_1	Active high during pattern exposure
TRIG_OUT_2	Active high pulse to indicate first pattern display

### 8.3.1.4 DLPC900 System Support Interfaces

#### 8.3.1.4.1 Reference Clock and PLL

The DLPC900 controller requires a 20-MHz 3.3-V external input from an oscillator. This signal serves as the DLPC900 chipset reference clock from which the majority of the interfaces derive their timing. This includes DMD interfaces and serial interfaces.

Refer to section [PCB Layout Guidelines for Internal Controller PLL Power](#) on PLL guidelines.

#### 8.3.1.4.2 Program Memory Flash Interface

The DLPC900 provides three external program memory chip selects for standard NOR-type flash:

- PM\_CSZ\_0 – flash device ( $\leq 128$  Mb)
- PM\_CSZ\_1 – dedicated CS for boot flash device ( $\leq 128$  Mb). Refer to the [Figure 23](#) for the memory layout of the boot flash.
- PM\_CSZ\_2 – flash device ( $\leq 128$  Mb)

Flash access timing is programmable up to 19 wait-states. [Table 23](#) contains the formulas to calculate the required wait-states for each of the parameters shown in [Figure 24](#) for a typical flash device. Refer to the DLPC900 Programmers Guide for details on how to set new wait-state values.

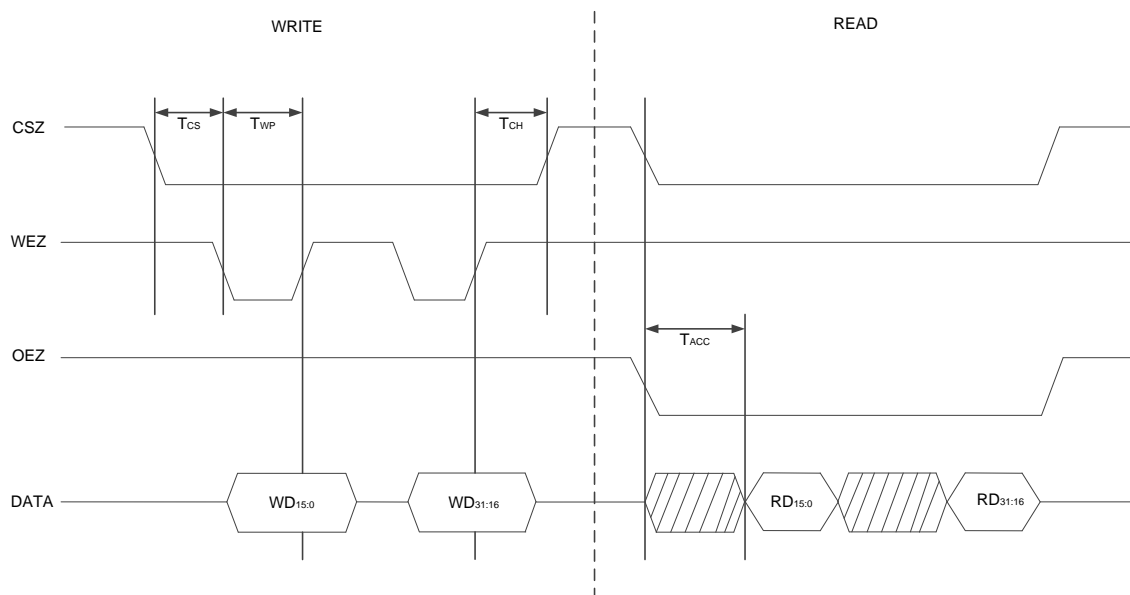
**Table 23. Flash Wait-States**

Parameter	Formula <sup>(1)</sup>	Default
T <sub>CS</sub> (CSZ low to WEZ low )	= Roundup((T <sub>CS</sub> + 5 ns) / 6.7 ns)	2
T <sub>WP</sub> (WEZ low to WEZ high)	= Roundup((T <sub>WP</sub> + 5 ns) / 6.7 ns)	11
T <sub>CH</sub> (WEZ high to CSZ high )	= Roundup((T <sub>CH</sub> + 5 ns) / 6.7 ns)	2
T <sub>ACC</sub> (CSZ low to Output Valid) <sup>(2)</sup>	= Roundup((T <sub>ACC</sub> + 5 ns) / 6.7 ns)	19
Maximum supported wait-states	19 (120ns) <sup>(3)</sup>	

(1) Assumes a maximum single direction trace length of 75 mm.

(2) In some flash device data sheets, the read access time may also be represented as T<sub>OE</sub>, T<sub>E</sub>, T<sub>RC</sub>, or T<sub>CE</sub>. Use the largest of these values to calculate the wait-states for the read access time.

(3) For each parameter.



**Figure 24. Flash Interface Timing Diagram**

### 8.3.1.4.3 DMD Interface

The DLPC900 controller provides the pattern data to the DMD over a double data rate (DDR) interface. [Table 24](#) describes the signals used for this interface.

**Table 24. Active Signals - DLPC900 to DMD Digital Data Interface**

SIGNAL NAME	DESCRIPTION
DDA(15:0)	DMD, LVDS interface channel A, differential serial data
DDB(15:0)	DMD, LVDS interface channel B, differential serial data
DCKA	DMD, LVDS interface channel A, differential clock
DCKB	DMD, LVDS interface channel B, differential clock
SCA	DMD, LVDS interface channel A, differential serial control
SCB	DMD, LVDS interface channel B, differential serial control

The DLPC900 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

**Table 25. Active Signals - DLPC900 to DMD Control Interface**

SIGNAL NAME	DESCRIPTION
DADOEZ	DMD output-enable (active low)
DADADDR(3:0)	DMD address
DADMODE(1:0)	DMD mode
DADSEL(1:0)	DMD select
DADSTRB	DMD strobe
DAD_INTZ	DMD interrupt (active low). This signal requires an external 1-K $\Omega$ pull-up and uses hysteresis.

The DLPC900 controls the micromirror control interface signals in a manner to ensure proper and reliable operation of the DMD.

## 9 Power Supply Recommendations

### 9.1 System Power Regulation

The PLLD\_VAD, PLLM1\_VAD, and PLLM2\_VAD power feeding internal PLLs must be derived from an isolated linear regulator with filter as recommended in [PCB Layout Guidelines for Internal Controller PLL Power](#) to minimize the AC noise component. [Figure 25](#)

It is acceptable to derive PLLD\_VDD, PLLM1\_VDD, PLLM2\_VDD, and PLLS\_VAD from the same regulator as the core VDDC, but they should be filtered as recommended in the [PCB Layout Guidelines for Internal Controller PLL Power](#).

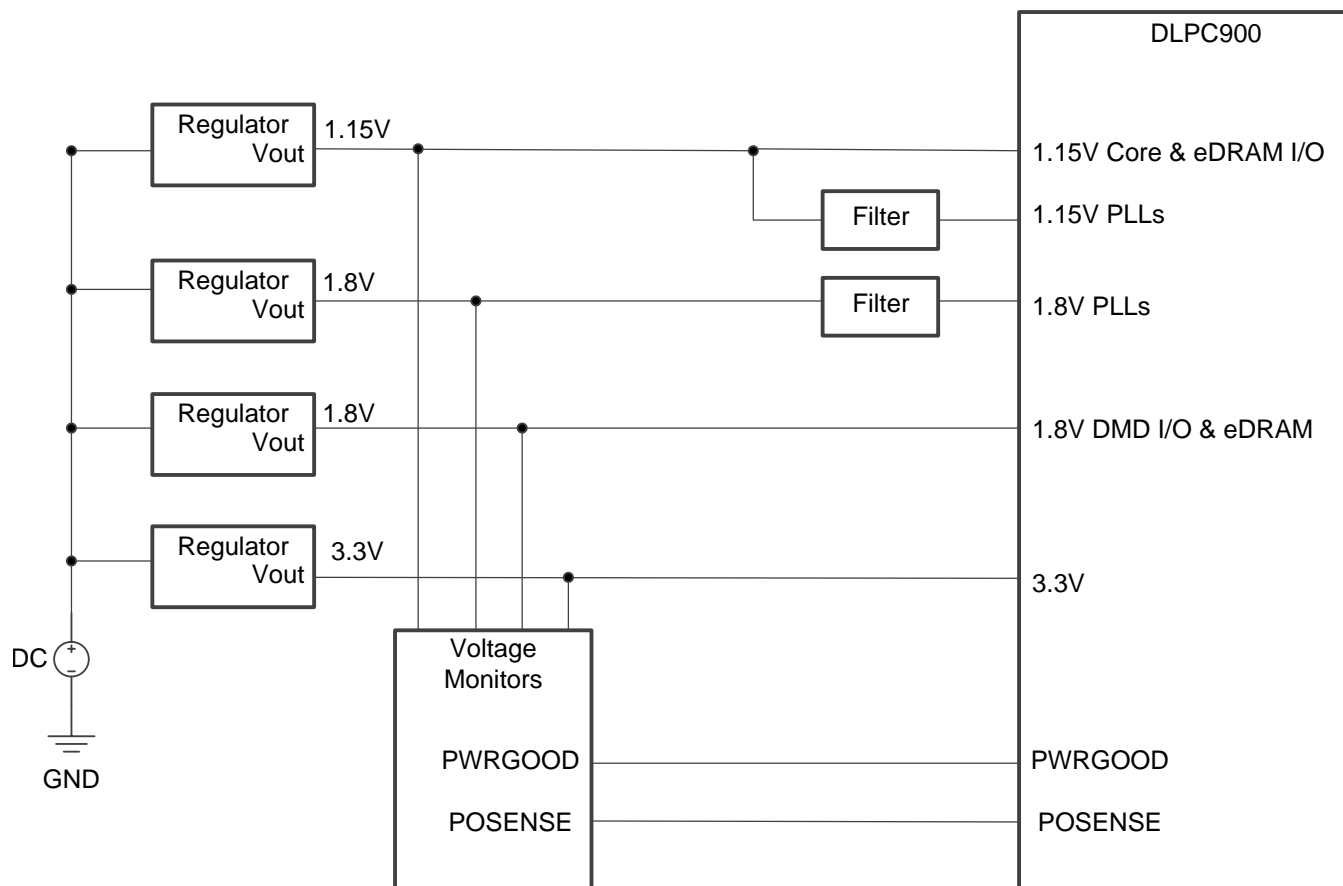


Figure 25. Power Regulation

#### 9.1.1 Power Distribution System

##### 9.1.1.1 1.15-V System Power

The DLPC900 can support a low-cost power delivery system with a single 1.15-V power source derived from a switching regulator. The main core should receive 1.15 V power directly from the regulator output, and the internal DLPC900 PLLs (PLLD\_VDD, PLLM1\_VDD, PLLM2\_VDD, and PLLS\_VAD) should receive individually filtered versions of this 1.15 V power. For specific filter recommendations, refer to the [PCB Layout Guidelines for Internal Controller PLL Power](#).

## System Power Regulation (continued)

### 9.1.1.2 1.8-V System Power

The DLPC900 power delivery system provides two independent 1.8-V power sources. One of the 1.8-V power sources should be used to supply 1.8-V power to the DLPC900 LVDS I/O and internal DRAM. Power for these functions should always be fed from a common source, which is recommended as a linear regulator. The second 1.8-V power source should be used (along with appropriate filtering as discussed in the [PCB Layout Guidelines for Internal Controller PLL Power](#)) to supply all of the DLPC900 internal PLLs (PLLD\_VAD, PLLM1\_VAD, and PLLM2\_VAD). To keep this power as clean as possible, a dedicated linear regulator is highly recommended for the 1.8-V power to the PLLs.

### 9.1.1.3 3.3-V System Power

The DLPC900 can support a low-cost power delivery system with a single 3.3-V power sources derived from a switching regulator. This 3.3-V power will supply all LVTTTL I/O and the crystal oscillator cell. The 3.3-V power should remain active in all power modes for which 1.15-V core power is applied.

## 9.2 System Environment and Defaults

### 9.2.1 DLPC900 System Power-Up and Reset Default Conditions

Following system power-up, the DLPC900 will perform a power-up initialization routine that will default the controller to its normal power mode in which all blocks are powered, all processor clocks will be enabled at their full rate and associated resets will be released. Most other clocks will default disabled with associated resets asserted until released by the processor. These same defaults will also be applied as part of all system reset events that occur without removing or cycling power. The 1.8-V power should be applied prior to releasing the reset so that the LVDS I/O and the internal embedded DRAM are enabled before the DLPC900 begins executing its system initialization routines.

## 9.3 System Power-Up Sequence

Although the DLPC900 requires an array of power supply voltages, for example, 1.15 V, 1.8 V, and 3.3 V, there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC900, as long as the system is held in reset during power supply sequencing. This is true for both power-up (reset controlled by POSENSE) and power-down (reset controlled by PWRGOOD) scenarios. Similarly, there is no minimum time between powering-up or powering-down the different supplies feeding the DLPC900. However, power-sequencing requirements are common for the devices that share the supplies with the DLPC900.

Power-sequencing recommendations to ensure proper operation are:

- 1.15-V core power should be applied whenever any I/O power is applied. This ensures the state of the associated I/O that are powered are set to a known state. Thus, applying core power first is recommended.
- All DLPC900 power should be applied before POSENSE is asserted to ensure proper power-up initialization is performed.

It is assumed that all DLPC900 power-up sequencing is handled by external hardware. It is also assumed that an external power monitor will hold the DLPC900 in system reset during power-up (that is, POSENSE = 0). During this time all controller I/O's will be tri-stated. The master PLL (PLLM1) will be released from reset upon the low-to-high transition of POSENSE, but the DLPC900 will be kept in for an additional 60 ms to allow the PLL to lock and stabilize its outputs. After this delay the DLPC900 internal resets will be deasserted, thus causing the processor to begin its boot-up routine.

[Figure 26](#) shows the recommended DLPC900 system power-up sequence of the regulators:



## System Power-Up Sequence (continued)

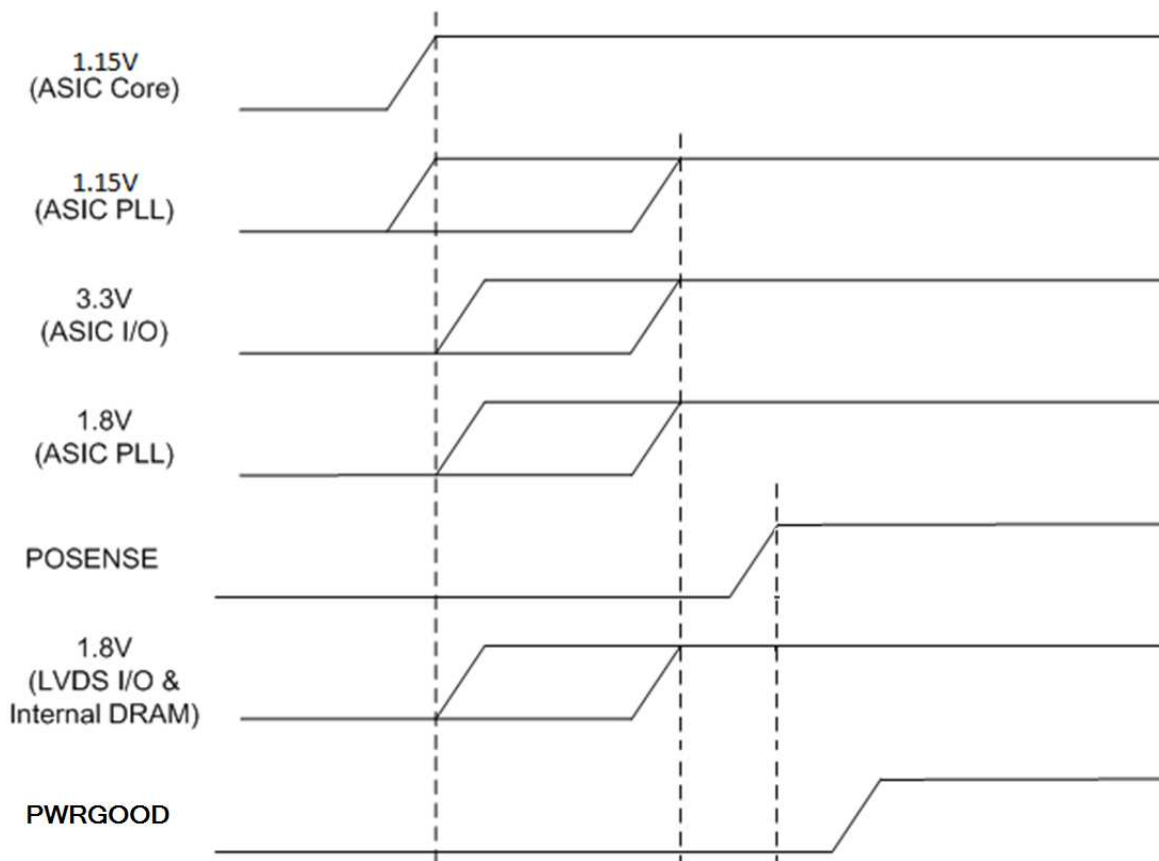


Figure 26. Power Sequencing

### 9.3.1 Power-On Sense (POSENSE) Support

It is difficult to set up a power monitor to trip exactly on the controller minimum supply voltage specification. Thus for practical reasons, the external power monitor generating POSENSE should target its threshold to 90% of the minimum supply voltage specifications and ensure that POSENSE remains low a sufficient amount of time for all supply voltages to reach minimum controller requirements and stabilize. The trip voltage for detecting the loss of power, as well as the reaction time to respond to a low voltage condition is not critical for POSENSE because PWRGOOD is used for this purpose. As such, PWRGOOD has critical requirements in these areas.

### 9.3.2 Power Good (PWRGOOD) Support

The PWRGOOD signal is defined as an early warning signal that alerts the controller a specified amount of time before the DC supply voltages drop below specifications. This warning lets the controller park the DMD mirrors and place the system into reset. See [Reset Timing Requirements](#).

### 9.3.3 5-V Tolerant Support

With the exception of USB\_DAT, the DLPC900 does not support any other 5V tolerant I/O. However, I<sup>2</sup>C typically have 5V requirements and special measures must be taken to support them. It is recommended that a 5V to 3.3-V level shifter be used.

It is strongly recommended that a 0.5-W external series resistance (of 22  $\Omega$ ) to limit the potential impact of a continuous short circuit between either USB D+ or USB D– to either Vbus, GND, the other data line, or the cable. For additional protection, also add an optional 200-mA Schottky diode from USB\_DAT to VDD33.

## 9.4 System Reset Operation

### 9.4.1 Power-Up Reset Operation

Immediately after a power-up event, DLPC900 hardware will automatically bring up the master PLL and place the controller in normal power mode. It will then follow the standard system reset procedure (see [System Reset Operation](#)).

### 9.4.2 System Reset Operation

Immediately after any type of system reset (power-up reset, PWRGOOD reset, watchdog timer time-out, and so forth), the DLPC900 automatically returns to normal power mode and returns to the following state:

- All GPIO will tri-state.
- The master PLL will remain active (it is only reset on a power-up reset) and most of the derived clocks will be active. However, only those resets associated with the DLPC900 processor and its peripherals will be released. (The DLPC900 firmware is responsible for releasing all other resets.)
- The DLPC900 associated clocks will default to their full clock rates (boot-up is at full speed).
- The PLL feeding the LVDS DMD interface (PLLD) will default to its power-down mode and all derived clocks will be inactive with corresponding resets asserted. (The DLPC900 firmware is responsible for enabling these clocks and releasing associated resets.)
- LVDS I/O will default to its power-down mode with tri-stated outputs.
- All resets output by the DLPC900 will remain asserted until released by the firmware (after boot-up).
- The DLPC900 processor will boot-up from external flash.

Once the DLPC900 processor boots-up, the DLPC900 firmware will:

- Configure the programmable DDR clock generator (DCG) clock rates (that is, the DMD LVDS interface rate)
- Enable the DCG PLL (PLLD) while holding divider logic in reset
- After the DCG PLL locks, the processor software will set DMD clock rates
- API software will then release DCG divider logic resets, which in turn, will enable all derived DCG clocks
- Release external resets

The LVDS I/O is reset by a system reset event and remains in reset until released by the DLPC900 firmware. Thus, the software is responsible for waiting until power is restored to these components before releasing reset.

## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 General PCB Recommendations

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity.

#### 10.1.2 PCB Layout Guidelines for Internal Controller PLL Power

The following are guidelines to achieve desired controller performance relative to internal PLLs:

The DLPC900 contains four PLLs (PLLM1, PLLM2, PLLD, and PLLS), each of which have a dedicated 1.15 V digital supply; three of these PLLs (PLLM1, PLLM2, and PLLD) have a dedicated 1.8 V analog supply. It is important to have filtering on the supply pins that covers a broad frequency range. Each 1.15 V PLL supply pin should have individual high frequency filtering in the form of a ferrite bead and a 0.1  $\mu\text{F}$  ceramic capacitor. These components should be located very close to the individual PLL supply balls. The impedance of the ferrite bead should far exceed that of the capacitor at frequencies above 10 MHz. The 1.15 V to the PLL supply pins should also have low frequency filtering in the form of an RC filter. This filter can be common to all the PLLs. The voltage drop across the resistor is limited by the 1.15 V regulator tolerance and the DLPC900 voltage tolerance. A resistance of 0.36  $\Omega$  and a 100  $\mu\text{F}$  ceramic are recommended. Figure 27 shows the recommended filter topology.

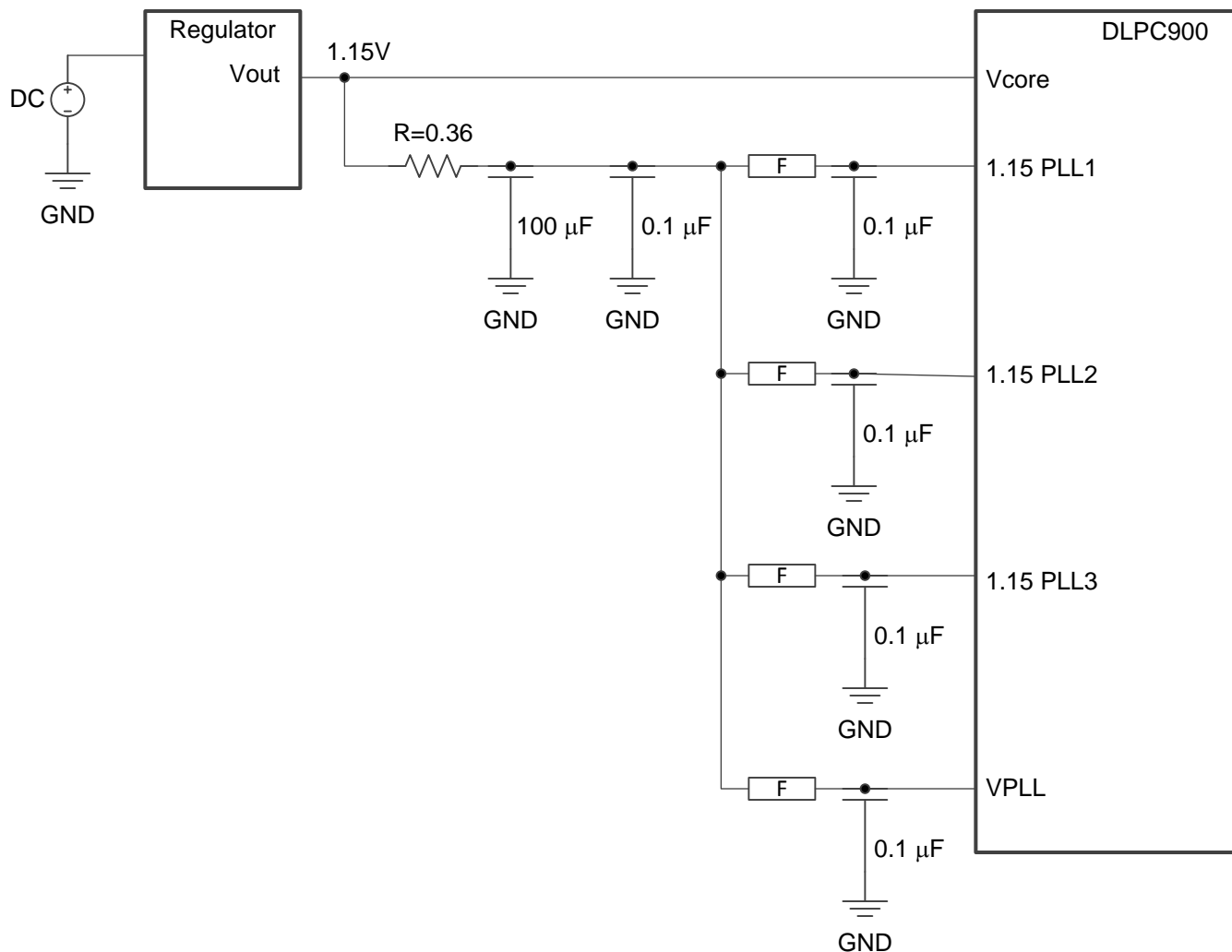
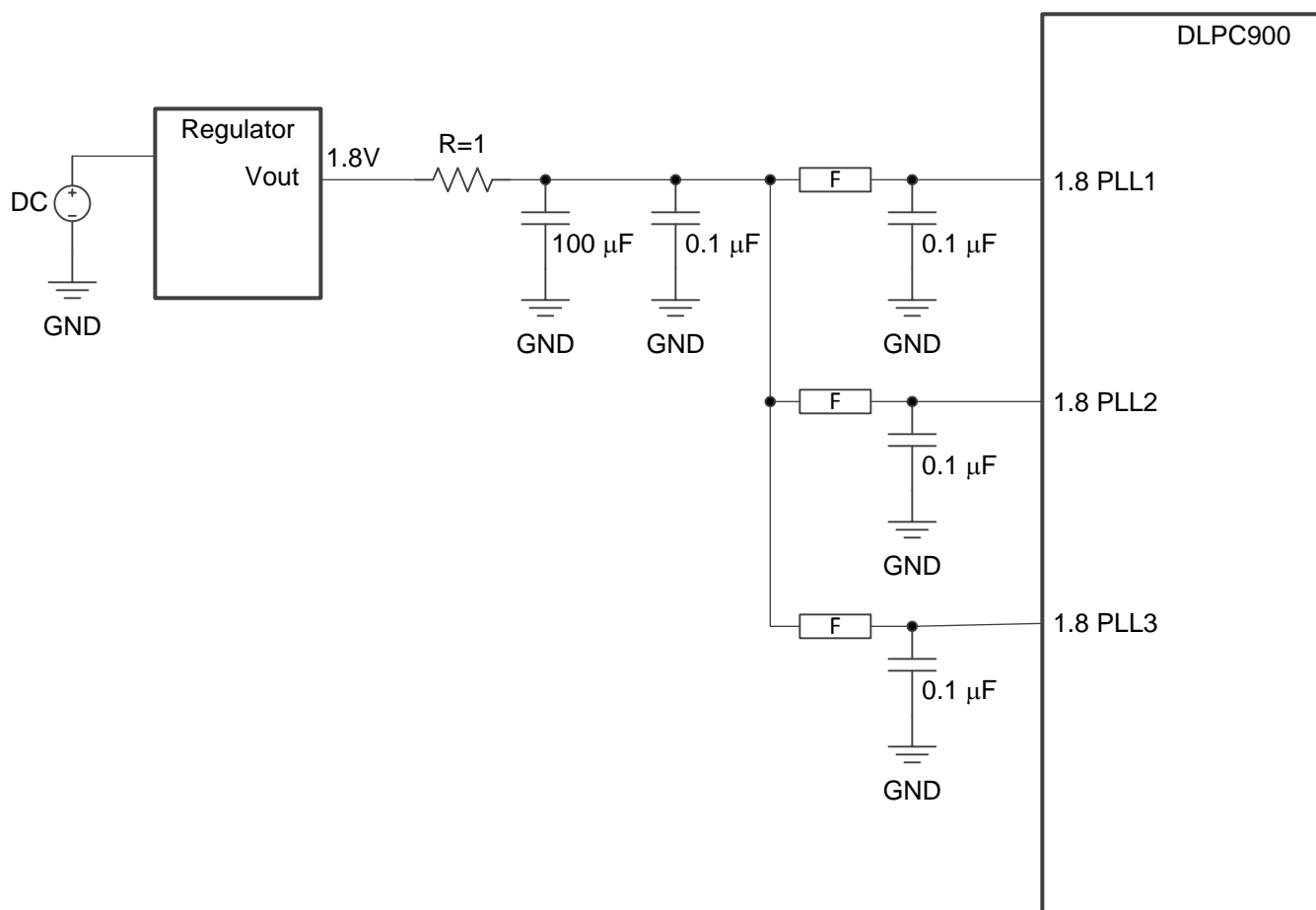


Figure 27. Recommended Filter Topology for PLL 1.15-V Supplies

## Layout Guidelines (continued)

The analog 1.8-V PLL power pins should have a similar filter topology as the 1.15 V. In addition, It is recommended that a dedicated linear regulator generates the 1.8 V. [Figure 28](#) shows the recommended filtering topology.



**Figure 28. Recommended Filter Topology for PLL 1.8-V Supplies**

When designing the overall supply filter network, care must be taken to ensure no resonance occurs. Specific care is required around the 1- to 2-MHz band, as this coincides with the PLL natural loop frequency.

## Layout Guidelines (continued)

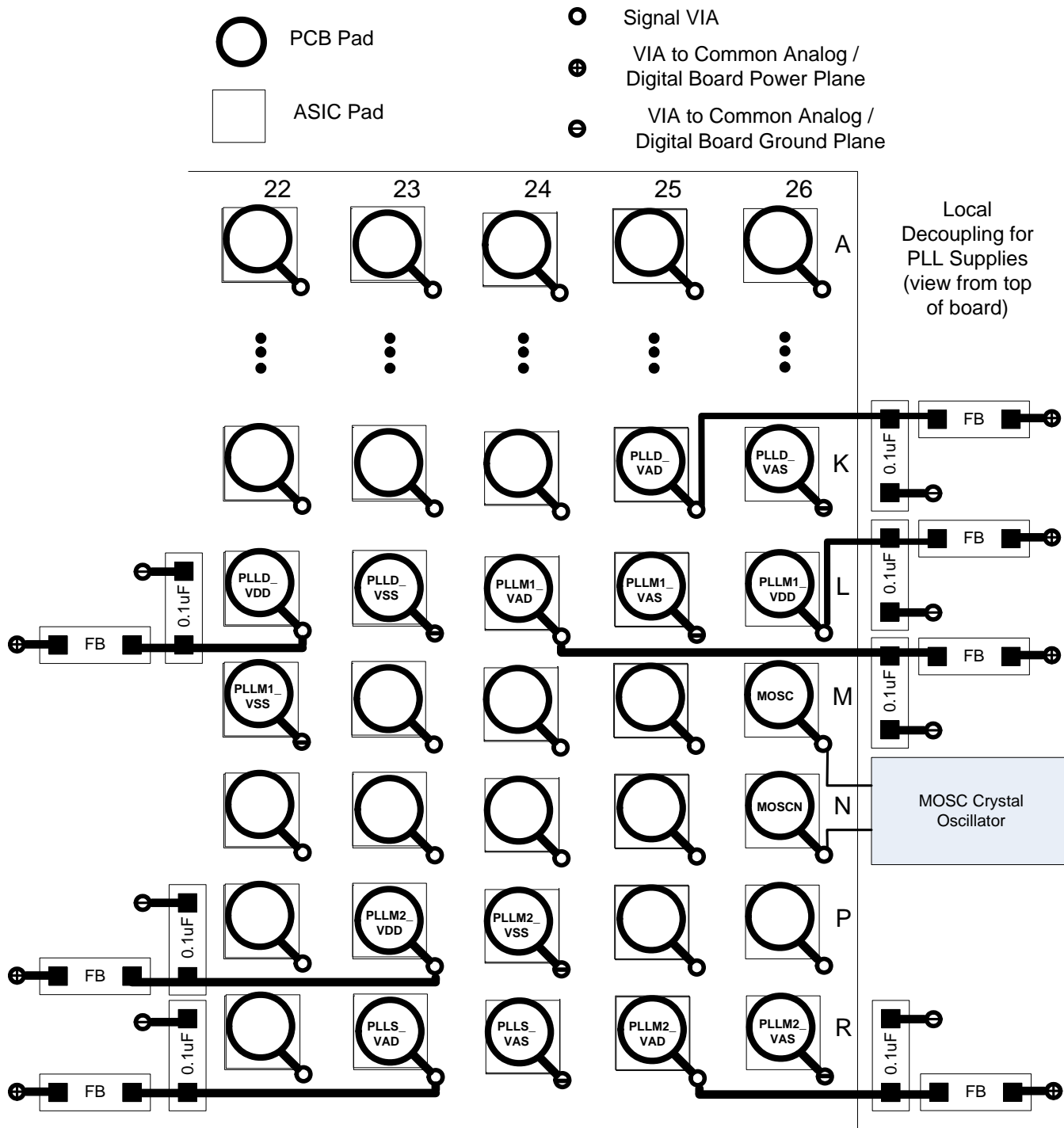


Figure 29. High Frequency Decoupling

## Layout Guidelines (continued)

High-frequency decoupling is required for 1.15-V and 1.8-V PLL supplies and should be provided as close as possible to each of the PLL supply package pins as shown in [Figure 29](#). Placing decoupling capacitors under the package on the opposite side of the board is recommended. High-quality, low-ESR, monolithic, surface-mount capacitors should be used. Typically, 0.1  $\mu$ F for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting, and thus, where possible, there should be no trace, allowing the via to butt up against the land. Additionally, the connecting trace should be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design.

### 10.1.3 PCB Layout Guidelines for Quality Video Performance

One of the most important factors to gain good performance is designing the PCB with the highest quality signal integrity possible. Here are a few recommendations:

1. Minimize the trace lengths between the video digital receiver and the DLPC900 port inputs.
2. Analog power should not be shared with the digital power directly.
3. Try to keep the trace lengths of the RGB as equal as possible.
4. Impedance matching between the digital receiver and the DLPC900 is important.

### 10.1.4 Recommended MOSC Crystal Oscillator Configuration

A recommended crystal oscillator configuration is shown in [Figure 30](#)

It is assumed that the external crystal oscillator will stabilize within 50 ms after stable power is applied.

**Table 26. Crystal Port Characteristics**

PARAMETER	NOMINAL	UNIT
MOSC-to-GND capacitance	1.5	pF
MOSCC-to-GND capacitance	1.5	pF

**Table 27. Recommended Crystal Configuration<sup>(1)</sup>**

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	20	MHz
Crystal temperature stability	$\pm 30$	PPM
Crystal frequency tolerance (including accuracy, temperature, aging, and trim sensitivity)	$\pm 100$	PPM
Crystal equivalent series resistance (ESR)	50 max	$\Omega$
Crystal load	20	pF
Crystal shunt load	7 max	pF
R <sub>S</sub> drive resistor (nominal)	100	$\Omega$
R <sub>FB</sub> feedback resistor (nominal)	1	M $\Omega$
C <sub>L1</sub> external crystal load capacitor (MOSC)	See <a href="#">Equation 1</a>	pF
C <sub>L2</sub> external crystal load capacitor (MOSCN)	See <a href="#">Equation 2</a>	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Typical drive level with the XSA020000FK1H-OCX crystal (ESR<sub>max</sub> = 40  $\Omega$ ) = 50  $\mu$ W

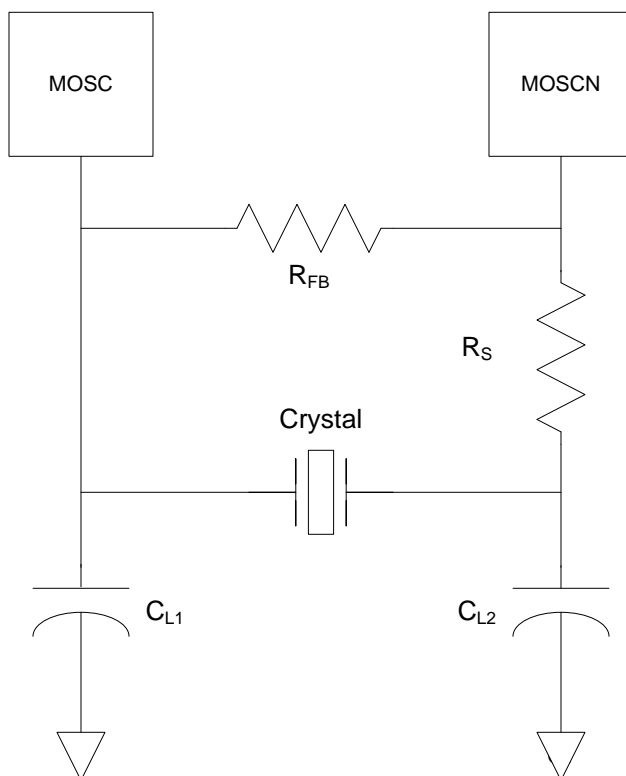
$$C_{L1} = 2 \times (C_L - C_{\text{Stray-MOSC}}) \quad (1)$$

$$C_{L2} = 2 \times (C_L - C_{\text{Stray-MOSCN}}) \quad (2)$$

where

- C<sub>L</sub> = Crystal load capacitance (Farads)
- C<sub>Stray-MOSC</sub> = Sum of package and PCB capacitance at the crystal pin associated with controller signal MOSC.

- $C_{\text{Stray-MOSCN}}$  = Sum of package and PCB capacitance at the crystal pin associated with controller signal MOSCN. (3)



**Figure 30. Crystal Oscillator Configuration**

### 10.1.5 Spread Spectrum Clock Generator Support

DLPC900 supports limited, internally controlled, spread spectrum clock spreading on the DMD interface. The purpose is to frequency-spread all signals on this high-speed external interface to reduce EMI emissions. Clock spreading is limited to triangular waveforms. The DLPC900 provides modulation options of 0%,  $\pm 0.5\%$ , and  $\pm 1.0\%$  (center-spread modulation).

### 10.1.6 GPIO Interface

The DLPC900 provides 9 software-programmable, general-purpose I/O pins. Each GPIO pin is individually configurable as either input or output. In addition, each GPIO output can be either configured as push-pull or open-drain. Some GPIO have one or more alternative use modes, which are also software configurable. The reset default for all GPIO is as an input signal. However, any alternative function connected to these GPIO pins, with the exception of general-purpose clocks and PWM generation, will be reset. When configured as open-drain, the outputs must be externally pulled-up (to the 3.3-V supply). External pull-up or pull-down resistors may be required to ensure stable operation before software can configure these ports.

### 10.1.7 General Handling Guidelines for Unused CMOS-type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended tying unused controller input pins through a pull-up resistor to its associated power supply or through a pull-down to ground unless noted in the Pin Functions. For controller inputs with an internal pull-up or pull-down resistor, it is unnecessary to add an external pull-up or pull-down unless specifically recommended. Internal pull-up and pull-down resistors are weak and should not be expected to drive the external line.

Unused output-only pins can be left open.

When possible, it is recommended to configure unused bidirectional I/O pins to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate resistor unless noted in the Pin Functions.

### 10.1.8 DMD Interface Considerations

High-speed interface waveform quality and timing on the DLPC900 controller (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

$$\text{Setup Margin} = (\text{controller output setup}) - (\text{DMD input setup}) - (\text{PCB routing mismatch}) - (\text{PCB SI degradation}) \quad (4)$$

$$\text{Hold-time Margin} = (\text{controller output hold}) - (\text{DMD input hold}) - (\text{PCB routing mismatch}) - (\text{PCB SI degradation}) \quad (5)$$

The PCB SI degradation is the signal integrity degradation due to PCB affects which includes such things as simultaneously switching output (SSO) noise, crosstalk, and intersymbol interference (ISI) noise.

DLPC900 I/O timing parameters, as well as DMD I/O timing parameters, can be easily found in their corresponding data sheets. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy-to-determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations may work, but should be confirmed with PCB signal integrity analysis or lab measurements.

PCB design: Refer to the [Figure 31](#).

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0-oz copper (1.2 mil)
Flex etch thickness (T):	0.5-oz copper (0.6 mil)
Single-ended signal impedance:	50 $\Omega$ ( $\pm 10\%$ )
Differential signal impedance:	100 $\Omega$ ( $\pm 10\%$ )

PCB stackup: Refer to the [Figure 31](#).

Reference plane 1 is assumed to be a ground plane for proper return path.

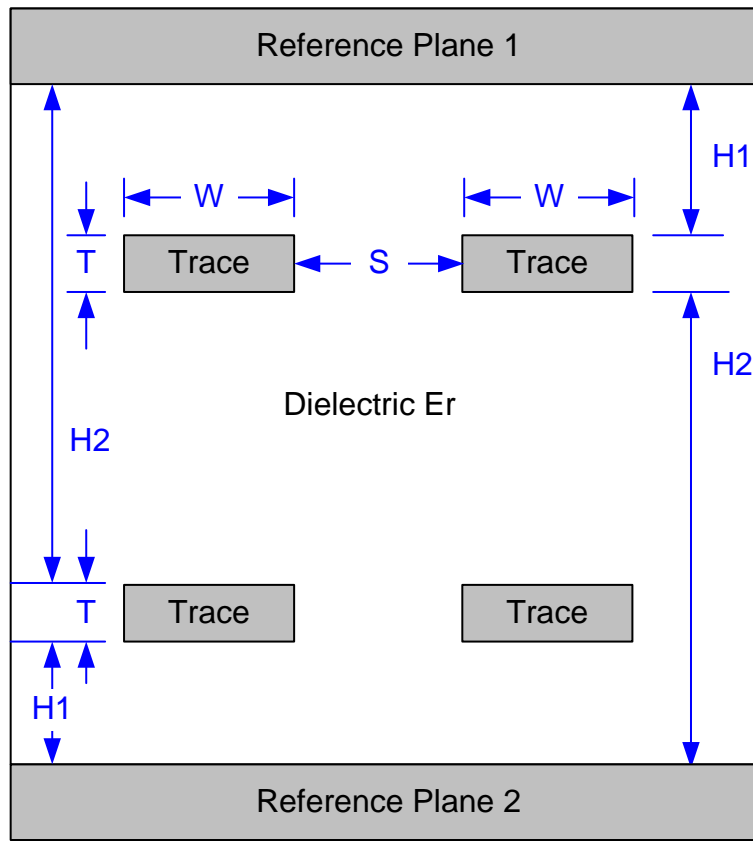
Reference plane 2 is assumed to be the I/O power plane or ground.

Dielectric FR4, (Er): 4.2 (nominal)

Signal trace distance to reference plane 1 (H1): 5.0 mil (nominal)

Signal trace distance to reference plane 2 (H2): 34.2 mil (nominal)





**Figure 31. PCB Stackup Geometries**

**Table 28. General PCB Routing (Applies to All Corresponding PCB Signals refer to the [Figure 31](#))**

Parameter	Application	Single-Ended Signals	Differential Pairs	Unit
Line width (W)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75 <sup>(1)</sup> (0.15)	mil (mm)
	PCB etch clocks	N/A	5.75 <sup>(1)</sup> (0.15)	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
Minimum line spacing to other signals (S)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements.

**Table 28. General PCB Routing (Applies to All Corresponding PCB Signals refer to the Figure 31) (continued)**

Parameter	Application	Single-Ended Signals	Differential Pairs	Unit
Maximum differential pair P-to-N length mismatch	Total data	N/A	12 (0.3)	mil (mm)
	Total clock	N/A	12 (0.3)	mil (mm)

**Table 29. DMD Interface Specific PCB Routing**

Signal Group length Matching				
Interface	Signal Group	Reference Signal	Max Mismatch	Unit
DMD (LVDS)	SCA_P/ SCA_N DDA_P_(15:0)/ DDA_N_(15:0)	DCKA_P/ DCKA_N	± 150 (± 3.81)	mil (mm)
DMD (LVDS)	SCB_P/ SCB_N DDB_P_(15:0)/ DDB_N_(15:0)	DCKB_P/ DCKB_N	± 150 (± 3.81)	mil (mm)

When routing the DMD Interface signals it is recommended to:

- Minimize the number of layer changes for Single-ended signals.
- Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

**Table 30. DMD Signal Routing Length<sup>(1)</sup>**

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Max signal routing length includes escape routing.

Stubs: Stubs should be avoided.

Termination Requirements: DMD interface: None – The DMD receiver is differentially terminated to 100 Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements should be used:

- Differential crosstalk: < 5%
- Differential impedance: 75 to 125 Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs should be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths.

These guidelines will produce a maximum PCB routing mismatch of 4.41 mm (0.174 inch) or approximately 30.4 ps, assuming 175 ps/inch FR4 propagation delay.

These PCB routing guidelines will result in approximately 25-ps system setup margin and 25-ps system hold margin for the DMD interface after accounting for signal integrity degradation as well as routing mismatch.

Both the DLPC900 output timing parameters and the DMD input timing parameters include timing budget to account for their respective internal package routing skew.

#### 10.1.8.1 Flex Connector Plating

Plate all the pad area on top layer of flex connection with a minimum of 35 and maximum 50 micro-inches of electrolytic hard gold over a minimum of 100 micro-inches of electrolytic nickel.

### 10.1.9 Thermal Considerations

The thermal limitation for the DLPC900 is that the maximum operating junction temperature ( $T_J$ ) must not be exceeded (this is defined in [Recommended Operating Conditions](#)). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC900, and power dissipation of surrounding components. The DLPC900 device package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature ( $T_A$ ) is provided primarily as a design target and is based on maximum DLPC900 power dissipation and  $R_{\theta JA}$  at 1 m/s of forced airflow, where  $R_{\theta JA}$  is the thermal resistance of the package as measured using a JEDEC-defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC900 PCB, and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However after the PCB is designed and the product is built, it is highly recommended thermal performance be measured and validated.

To do this, the top-center case temperature should be measured under the worse case product scenario (max power dissipation, max voltage, max ambient temp) and validated not to exceed the maximum recommended case temperature ( $T_C$ ). This specification is based on the measured  $\phi_{JT}$  for the DLPC900 package and provides a relatively accurate correlation to junction temperature. Care must be taken when measuring this case temperature to prevent accidental cooling of the package surface. It is recommended to use a small (approximately 40 gauge) thermocouple. The bead and the thermocouple wire should be covered with a minimal amount of thermally conductive epoxy and contact the top of the package. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

### 10.1.10 PCB Design Standards

PCB designed and built in accordance with the following industry specifications:

**Table 31. Industry Design Specification**

Industry Specification	Applicable To
IPC-2221 and IPC2222, Type 3, Class X, at Level B producibility	Board Design
IPC-6011 and IPC-6012, Class 2	PWB Fabrication
IPC-SM-840, Class 3, Color Green	Finished PWB Solder mask
UL94V-0 Flammability Rating and Marking	Finished PWB
UL796 Rating and Marking	Finished PWB

### 10.1.11 Signal Layers

The PCB signal layers should follow typical good practice guidelines including:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first.
- Pin swapping on components is not allowed.

The PCB should have a solder mask on the top and bottom layers. The mask should not cover the vias.

- Except for fine pitch devices (pitch  $\leq$  0.032 inches), the copper pads and the solder mask cutout should be of the same size.
- Solder mask between pads of fine pitch devices should be removed.
- In the BGA package, the copper pads and the solder mask cutout should be of the same size.

### 10.1.12 Trace Widths and Minimum Spacing

BGA escape routing can be routed with 4mils width and 4 mils spacing, as long as the escape nets are less than 1 inch long, to allow 2 traces fit between vias. After signals escape the BGA field, trace width should be widened to achieve the desired impedance and spacing.

All single-ended 50ohm signal must have a minimum spacing of 10mils relative to other signals. Other special trace spacing requirements are listed in [Table 32](#)

**Table 32. Traces Widths and Minimum Spacing**

Signal on Pin	Minimum Width	Minimum Space
VDDC, VDD18, VDD33	0.020	0.015
GND	0.015 <sup>(1)</sup>	0.005
PLLS_VAD, PLLM2_VDD, PLLD_VDD, PLLM1_VDD, PLLM1_VAD, PLLM2_VAD, PLLD_VAD	0.012 (keep length less than 260mils)	0.015
MOSCP, OCLKA		0.020 <sup>(2)</sup>
SCA_(P,N), DDA_(P,N)_(15:00), SCB_(P,N), DDB_(P,N)_(15:00), DCKA_(P,N), DCKB_(P,N)		0.030 <sup>(2)</sup>
USB_DAT_(P,N)		0.030 <sup>(2)</sup>

(1) Make width of GND trace as wide as the pin it is connected to, when possible.

(2) Trace spacing of these signals/signal-pairs relative to other signals

### 10.1.13 Trace Impedance and Routing Priority

For best performance, it is recommended that the trace impedance for differential signals as in [Table 33](#).

All signals should be 50 ohms controlled impedance unless otherwise noted in [Table 33](#).

**Table 33. Trace Impedance**

Signal on Pin	Differential Impedance
DCKA_(P,N)	100 $\Omega$ $\pm$ 10%
SCA_(P,N)	
DDA_(P,N)_(15:00)	
DCKB_(P,N)	100 $\Omega$ $\pm$ 10%
SCB_(P,N)	
DDB_(P,N)_(15:00)	
USB_DAT_(P,N)	90 $\Omega$ $\pm$ 10%
USB_(P,N)	
All other Differential Signals	100 $\Omega$ $\pm$ 10%

[Table 34](#) lists the signals' routing priority assignment.

**Table 34. Routing Priority**

Signal on Pin	Priority
DCKA_(P,N) SCA_(P,N) DDA_(P,N)_(15:00) DCKB_(P,N) SCB_(P,N) DDB_(P,N)_(15:00)	1 <sup>(1)(2)(3)</sup>
USB_(P,N) USB_DAT_(P,N)	2 <sup>(1)</sup>
P1(A,B,C)(9:0), P2(A,B,C)(9:0), P_CLK1, P_CLK2, P_CLK3, P_DATEN1, P_DATEN2, P1_VSYNC, P2_VSYNC, P1_HSYNC, P2_HSYNC	3 <sup>(1)(2)(3)</sup>
OCLKA, MOSCP	4 <sup>(4)</sup>

(1) Refer to Table 8 for length matching requirement

(2) Switching layer should not be done except at the beginning and end of the trace

(3) Maximum routing length of 2 inches for each signal/pair, includes escape routing

(4) Keep routing length under 0.35 inches

#### 10.1.14 Power and Ground Planes

For best performance, the following are recommendations:

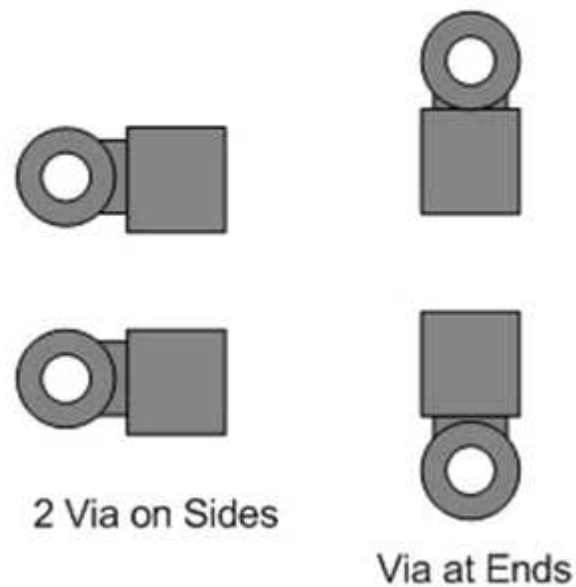
- Solid ground planes between each signal routing layer
- Two solid power planes for voltages.
- Power and ground pins should be connected to these planes through a via for each pin
- All device pin and via connections to these planes should use a thermal relief with a minimum of four spokes
- Trace lengths for the component power and ground pins should be minimized to 0.03 inches or less
- Vias should be spaced out to avoid forming slots on the power planes
- High speed signals should not cross over a slot in the adjacent power planes
- Vias connecting all the digital layers should be placed around the edge of the rigid PCB regions 0.03 inches from the board edges with 0.1 inch spacing prior to routing
- Placing extra vias is not required if there are sufficient ground vias due to normal ground connections of devices
- All signal routing and signal vias should be inside the perimeter ring of ground vias

#### 10.1.15 Power Vias

Power and Ground pins of each component shall be connected to the power and ground planes with a via for each pin. Avoid sharing vias to the power plane among multiple power pins, where possible. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100"). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. The minimum spacing between vias shall be 0.050" to prevent slots from being developed on the ground plane.

#### 10.1.16 Decoupling

Decoupling capacitors must be located as near as possible to the DLPC900 voltage supply pins. Capacitors should not share vias. The DLPC900 power pins can be connected directly to the decoupling capacitor (no via) if the trace is less than 0.03". Otherwise the component should be tied to the voltage or ground plane through a separate via. All capacitors should be connected to the power planes with trace lengths less than 0.05". Try to mount decoupling capacitors connecting to power rail VDD11 (1.15 V) using "via on sides" geometry as shown below in [Figure 32](#). If "via on the side" is not possible, 1.15 V decoupling capacitors can be mounted using "via at ends" method, providing traces between the vias and decoupling capacitors' pads be as short and wide (at least 15mils wide) as possible.



**Figure 32. Decoupling Via Placement**

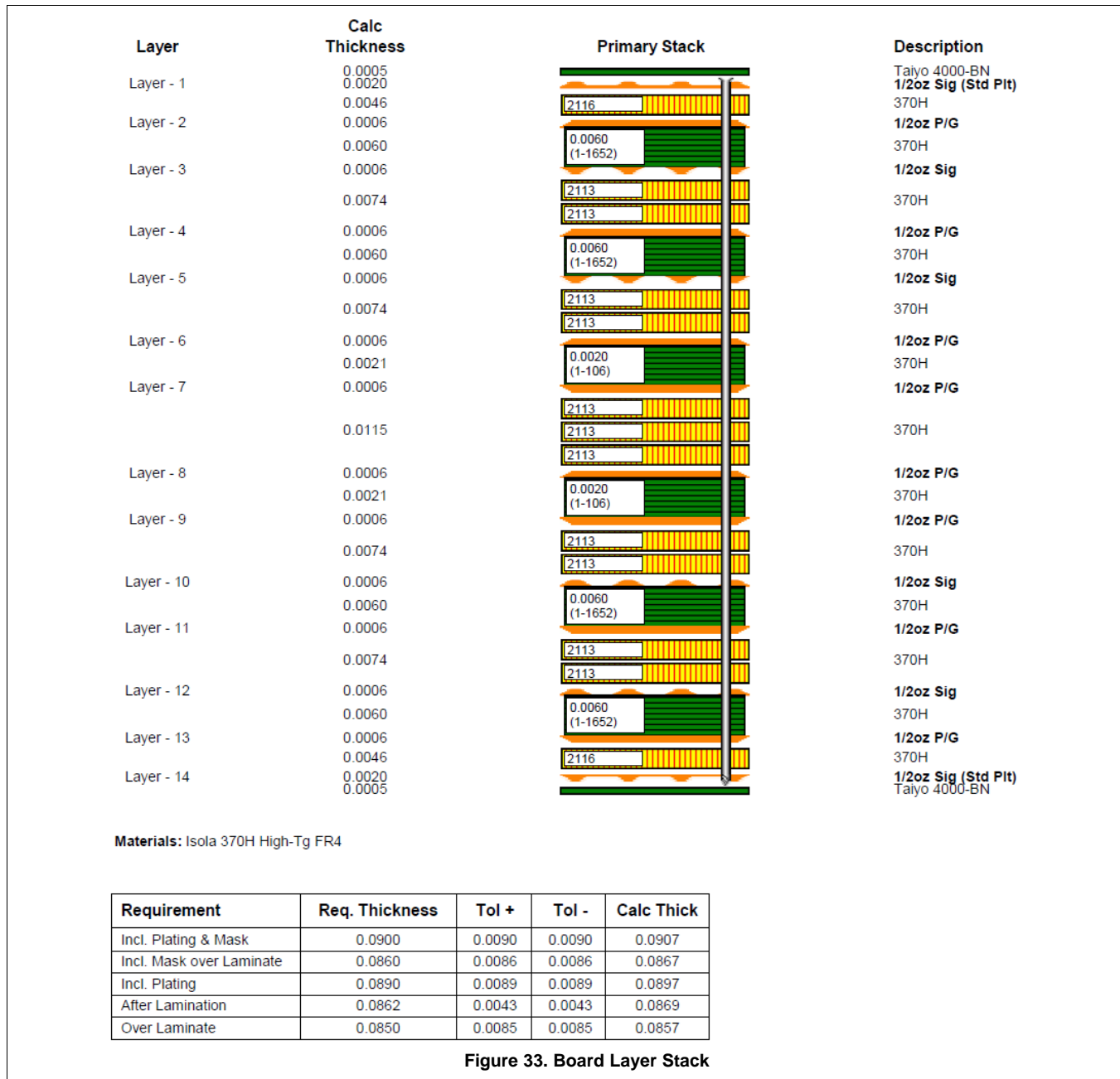
#### 10.1.17 Fiducials

Fiducials for automatic component insertion should be placed on the board according to the following guidelines or on recommendation from manufacturer:

















- Fiducials for optical auto insertion alignment shall be placed on three corners of both sides of the PCB
- Fiducials should be 0.050" copper with 0.100" cutout (antipad).

## 10.2 Layout Example

The DLP® LightCrafter™ 9000 EVM PCB is targeted at 14 layers with layer stack up shown in Figure 33. The PCB layer stack may vary depending on system design. However, careful attention is required to meet design considerations. Layers 1 and 14 should consist of the components layers. Layers 2, 4, 6, 9, 11, and 13 should consist of solid ground planes. Layers 7 and 8 should consist of solid power planes. Layers 1, 3, 5, 10, 12, and 14 should be used as the primary routing layers. Routing on external layers should be less than 0.25 inches for priority one and two signals. Refer to the Table 34 for signal priority groups. Board material should be FR-370HR or similar. PCB should be designed for lead-free assembly with the stackup geometry shown in Figure 33 and Figure 34.



**Layout Example (continued)**

Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1  Surface MS	L1	-	0.0068	-	-	50	5.0	50.20
	-	-	-	-	L2			
2  EC Microstrip	L1	-	0.0055	0.0110	-	90	9.0	89.55
	-	-	0.0055	-	L2			
3  EC Microstrip	L1	0.00475	0.00475	0.0120	-	100	10.0	100.27
	-	0.00475	0.00475	-	L2			
4  Stripline	L3	-	0.0057	-	L2	50	5.0	49.34
	-	-	-	-	L4			
5  EC Stripline	L3	-	0.0054	0.0110	L2	90	9.0	89.75
	-	-	0.0054	-	L4			
6  EC Stripline	L3	0.00475	0.00475	0.0120	L2	100	10.0	99.03
	-	0.00475	0.00475	-	L4			
7  Stripline	L5	-	0.0057	-	L4	50	5.0	49.34
	-	-	-	-	L6			
8  EC Stripline	L5	-	0.0054	0.0110	L4	90	9.0	89.75
	-	-	0.0054	-	L6			
9  EC Stripline	L5	0.00475	0.00475	0.0120	L4	100	10.0	99.03
	-	0.00475	0.00475	-	L6			
10  Stripline	L10	-	0.0057	-	L9	50	5.0	49.34
	-	-	-	-	L11			
11  EC Stripline	L10	-	0.0054	0.0110	L9	90	9.0	89.75
	-	-	0.0054	-	L11			
12  EC Stripline	L10	0.00475	0.00475	0.0120	L9	100	10.0	99.03
	-	0.00475	0.00475	-	L11			
13  Stripline	L12	-	0.0057	-	L11	50	5.0	49.34
	-	-	-	-	L13			
14  EC Stripline	L12	-	0.0054	0.0110	L11	90	9.0	89.75
	-	-	0.0054	-	L13			
15  EC Stripline	L12	0.00475	0.00475	0.0120	L11	100	10.0	99.03
	-	0.00475	0.00475	-	L13			
16  Surface MS	L14	-	0.0068	-	L13	50	5.0	50.20
	-	-	-	-	-			

**Figure 34. Board Trace Geometry**

Refer to section Device and Documentation Support for a complete set of documentation for the DLP LightCrafter 9000 EVM reference design.



## 11 Device and Documentation Support

The following documents contain additional information related to the use of the DLPC900 device.

**Table 35. Related Documents**

DOCUMENT	TI LITERATURE NUMBER
DLP6500FLQ DMD Data Sheet	<a href="#">DLPS040</a>
DLP6500FYE DMD Data Sheet	<a href="#">DLPS053</a>
DLP9000 DMD Data Sheet	<a href="#">DLPS036</a>
DLPC900 Programmer's Guide	<a href="#">DLPU018</a>
DLP LightCrafter 6500 and 9000 EVM User's Guide	<a href="#">DLPU028</a>
Reference Design Documentation	<a href="#">DLPLCR6500</a> <a href="#">DLPLCR9000</a>

### 11.1 Device Support

#### 11.1.1 Video Timing Parameter Definitions

**Active Lines Per Frame (ALPF)** Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.

**Active Pixels Per Line (APPL)** Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.

**Horizontal Back Porch (HBP) Blanking** Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.

**Horizontal Front Porch (HFP) Blanking** Number of blank pixel clocks after the last active pixel but before Horizontal Sync.

**Horizontal Sync (HS)** Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

**Total Lines Per Frame (TLPF)** Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).

**Total Pixel Per Line (TPPL)** Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).

**Vertical Back Porch (VBP) Blanking** Number of blank lines after vertical sync but before the first active line.

**Vertical Front Porch (VFP) Blanking** Number of blank lines after the last active line but before vertical sync.

**Vertical Sync (VS)** Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

## Device Support (continued)

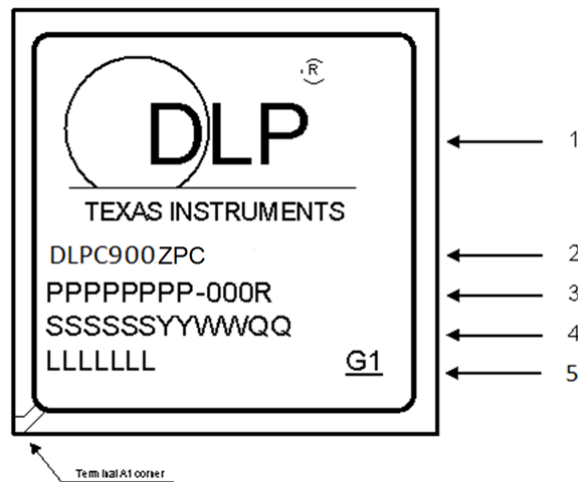
### 11.1.2 Device Nomenclature

**Table 36. Part Number Cross-Reference**

TI Part Number <sup>(1)</sup>	Description	Manufacturer's Reference Name	Manufacturer's Process Control Number
DLPC900ZPC-X	Engineering Samples – DLPC900	DLPC900	T6WH0XBG-0001W2N
DLPC900ZPC	Production Units – DLPC900	DLPC900	T6WH0XBG-0001W2N

(1) Engineering prototype samples are marked with an **X** suffix appended to the TI part number.

### 11.1.3 Device Markings



#### Marking Definitions:

- Line 1: DLP logo
- Line 2: DLP device name
- Line 3: Foundry part number
- Line 4: SSSSSSSYYWW-QQ package assembly information
  - SSSSSS: Manufacturing site
  - YYWW: Date code (YY = Year :: WW = Week)
  - QQ: Qualification level option – Engineering samples are marked in this field with the suffix –ES. For example, TAIWAN0324-ES would be engineering samples built in Taiwan the 24<sup>th</sup> week of 2003
- Line 5: LLLLLLL G1 manufacturing lot code for semiconductor wafers and lead-free solder ball marking
  - LLLLLLL: Manufacturing lot code
  - G1: Lead-free solder balls consisting of SnAgCu

## 11.2 Trademarks

LightCrafter is a trademark of Texas Instruments.  
DLP is a registered trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC900ZPC	ACTIVE	BGA	ZPC	516	1	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-255C-168 HR			<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

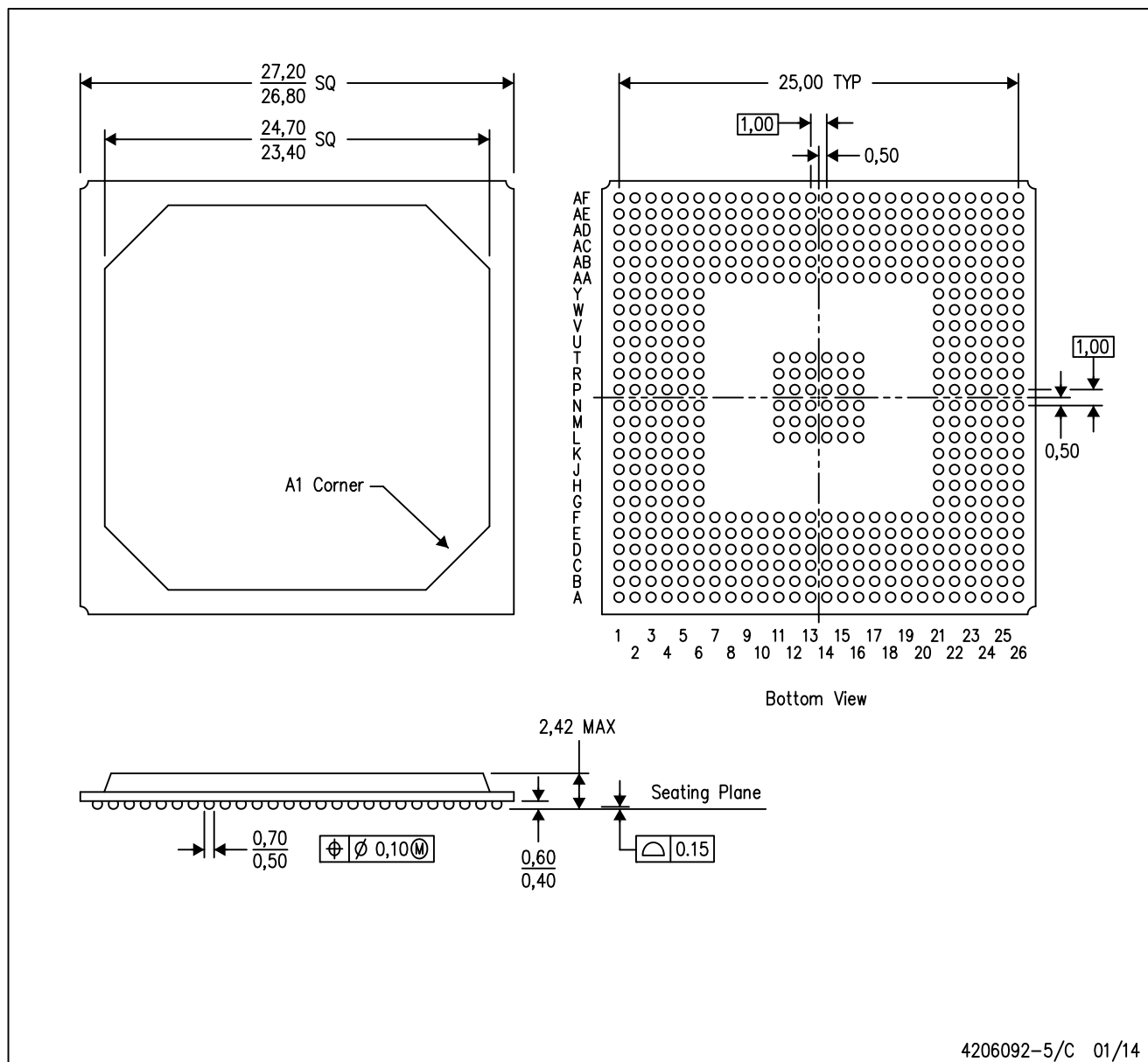
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ZPC (S-PBGA-N516)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. This package is Pb-free.

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